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Master Thesis

MBE growth and characterization of InAs/GaSb core/shell nanowire arrays

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Abstract

III-V semiconductor compounds InAs and GaSb are almost lattice matched and when in contact, the heterostructure appears to have a broken gap alignment at their interface[1]. In a core/shell nanowire (NW) geometry, these particularities make this combination interesting for low power electronic devices (Tunneling Field Effect Transistors) as well as the study of fundamental physical properties such as quantum effects arising due to electron interference. This thesis reports on the MBE growth as well as the structural and electrical characterization of InAs/GaSb NW arrays.

For the growth, a Si(111) substrate is covered with a thin thermal SiO_2 film in which two-dimensional, periodic arrays of nano-sized holes are patterned. The InAs NW growth is optimized regarding the yield and morphology of the wires. Substrate preparation thereby is crucial for achieving a high NW yield. The subsequent growth of the GaSb shell has been investigated and optimum growth conditions have been achieved. The effect of doping of the GaSb shell and substrate temperature, during shell deposition, is also studied. NW morphology and structural characteristics have been investigated. The small lattice mismatch between InAs and GaSb combined with the one-dimensional geometry result in a misfit dislocation free core–shell NW hetero-interface.

Post-growth, the GaSb shell is etched from part of the NW to have access to the InAs core in order to study the transport at the hetero-junction. Dry and wet etching techniques provide different results, both of which can be used for fabricating NW devices. Metallic contacts have been fabricated on different parts of these partially etched core/shell NWs as well as on non-etched wires. This process is optimized for the dimensions of these core/shell NWs with respect to reproducibility.

Electrical characterization includes gate dependent measurements, which have been carried out at room temperature as well as at low temperatures down to 1.5 K using a cryogenic setup. Magneto-transport measurements are used to probe electron transport in these nanoscopic systems. Characterization therefore includes the observation of quantum mechanical electron interference effects probed at different temperatures and different angles of the magnetic field with respect to the NW axis. Analysis on this data includes approximations of typical figures of merit like the phase coherence length or the elastic mean free path but also includes a proper analysis of the size and possible locations of the electron interference loops.

Contents

Introduction

Optimization, for better or worse, has become an inherent part of our lifestyle. Everyone is contributing in their own way towards optimization of something. Science, however, is one of the fields which offers us a chance to look beyond optimization and work on something solely to quench one's curiosity. A good analogy to this line of thought is the study of InAs/GaSb nanowires (NWs).

Exploiting the quantum mechanical effects that govern the behavior of a material at the microscopic dimensions forms the basis of solid-state physics. The same quantum mechanical effects that are the reason for the wave functions of conduction electrons to incorporate the periodicity of a lattice and result in distinct charge transport phenomenon, are also responsible for the stagnation caused in lowering device dimensions to a dimension where phase coherence effects and electron interference effects become detrimental to charge transport.

III-V semiconductors offer a large variety of materials that are suitable for electronic and opto-electronic applications and combining this with the possibility to fabricate structures at a scale less than a micrometer allows for better control over their intrinsic properties such as the carrier mobility. They also allow for the possibility form hetero-structures with the flexibility to combine various materials. Integration of these materials onto Si is essential, however, very few materials show a small lattice mismatch with Si. Dislocations due to a high lattice mismatch can be avoided by modifying layer epitaxial growth to a vertical NW, effectively reducing the dislocations by suppressing lateral growth. Integration of multiple materials in the NW geometry is easier than in a layer system due to higher critical dimensions required for a strain relaxed growth. NWs are also highly interesting since they can be effectively used as a conductive channel in a device at the nanometer scale.

For a transistor like device where a switching mechanism is desired, the electron spin or phase can be incorporated to govern the switching. The material system with InAs/GaSb exhibits a lattice mismatch of 0.6% and is theoretically predicted to have a type III broken gap alignment which may result in a semi-metallic behavior. InAs/GaSb core/shell NWs have recently been reported to exhibit negative differential resistance (NDR), the characteristic of a tunneling diode. Controlling the NDR with a gate voltage effectively results in its application as a tunneling field effect transistor (TFET)[2, 3, 4, 5, 6]. Moreover, theoretical simulations have predicted the existence of a negative band gap and even a mini gap that results from the hybridization of electrons and holes in InAs and GaSb respectively[7, 8]. This is promising in the search for topological insulator behavior since these hybridization gaps have a direct dependence on the dimensions of the structure which can be tailored accordingly, especially in the NW geometry.

In this regard, this work is dedicated to optimizing the self-catalyzed selective area epitaxy (SAE) of InAs/GaSb core/shell NWs on Si(111) using molecular beam epitaxy as well as characterizing them electrically. The first chapter of the thesis gives a brief overview of the theoretical and technical background used throughout the work. The second chapter demonstrates the selective area epitaxy of InAs NW and hence InAs/GaSb core/shell NW arrays. The effect and optimization of substrate preparation for SAE and growth parameters such as doping the GaSb shell and substrate temperature are discussed. The processing of NW device fabrication using NWs with a partially etched GaSb shell is presented in the third chapter. Here, the selective etching of the NW shell is established first and then the process of metal deposition on the NW for device fabrication is carried out next. In the fourth chapter, DC characterization conducted on NWs with a partially etched shell and non-etched shell is analyzed. For more clarity with regard to the charge transport contribution from both materials, temperature and angle dependent magneto-transport measurements are conducted on InAs/GaSb core/shell NWs. Finally, the results are summarized and an outlook for future device processing and possible further investigations that could be conducted is presented in the last chapter.

Theory

“If you only read the books that everyone else is reading, you can only think what everyone else is thinking.”

- Haruki Murakami

1 Theoretical and technical background

1.1 Band structure of InAs/GaSb core/shell nanowires

In order to study the transport properties of InAs/GaSb core/shell NWs, it is essential to understand the band structure of this system. Different materials exhibit different lattice constants and this induces a strain when they are in contact. The band alignment of these materials is then a result of the modifications caused due to the strain as well as the ratio of the core and the radius rather than the absolute values[9]. Fig. 1.1 (a) displays the different types of band alignments for core/shell semiconductor NWs depending on the materials in question[1, 10]. These are calculated for III-V NWs with a zinc-blende structure oriented along the [111] direction with a hexagonal cross-section, under the assumption that most NWs grown using vapour-solid-liquid methods exhibit these properties[1]. In reality however, most III-V NWs exhibit polytypism i.e., zinc blende (ZB) as well as wurtzite (WZ) structure[11].

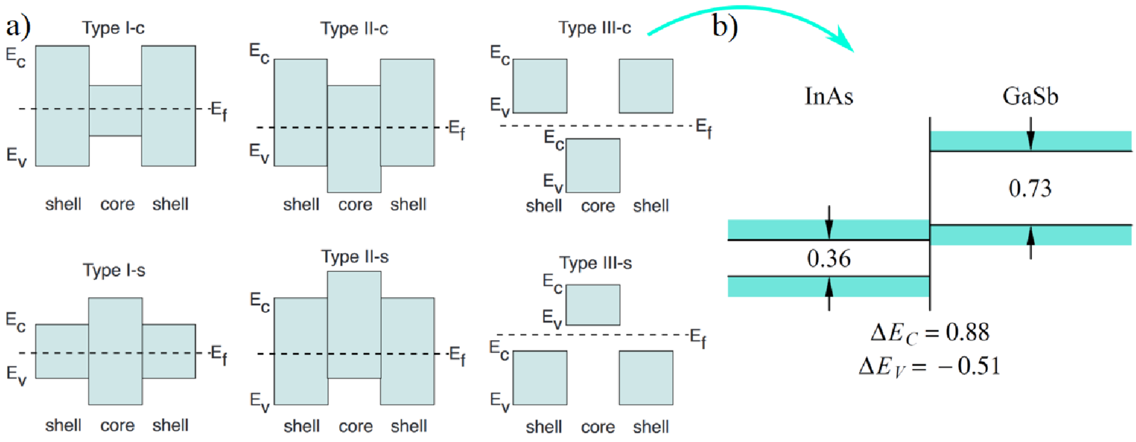


Figure 1.1: *Different possible band structures for core/shell NW structures(1). E_c, E_v and E_f denote the conduction band minima, valence band maxima and the Fermi energy respectively[1, 10].*

Here, E_c and E_v denote the conduction band minimum and the valence band maximum, respectively, and E_f denotes the Fermi level. The blue bands effectively display the energy band gaps for the core and shell as labeled. The '-s' and '-c' annotations differentiate the case where the E_c of the shell lies below that of the core and vice versa. The material system InAs/GaSb core/shell NW exhibits a type III-c band alignment. This is a so-called broken gap structure with the E_c of InAs lying below the E_v of GaSb. The expected band gap energies for this system are given in units of electron Volts (eV) and are displayed in the

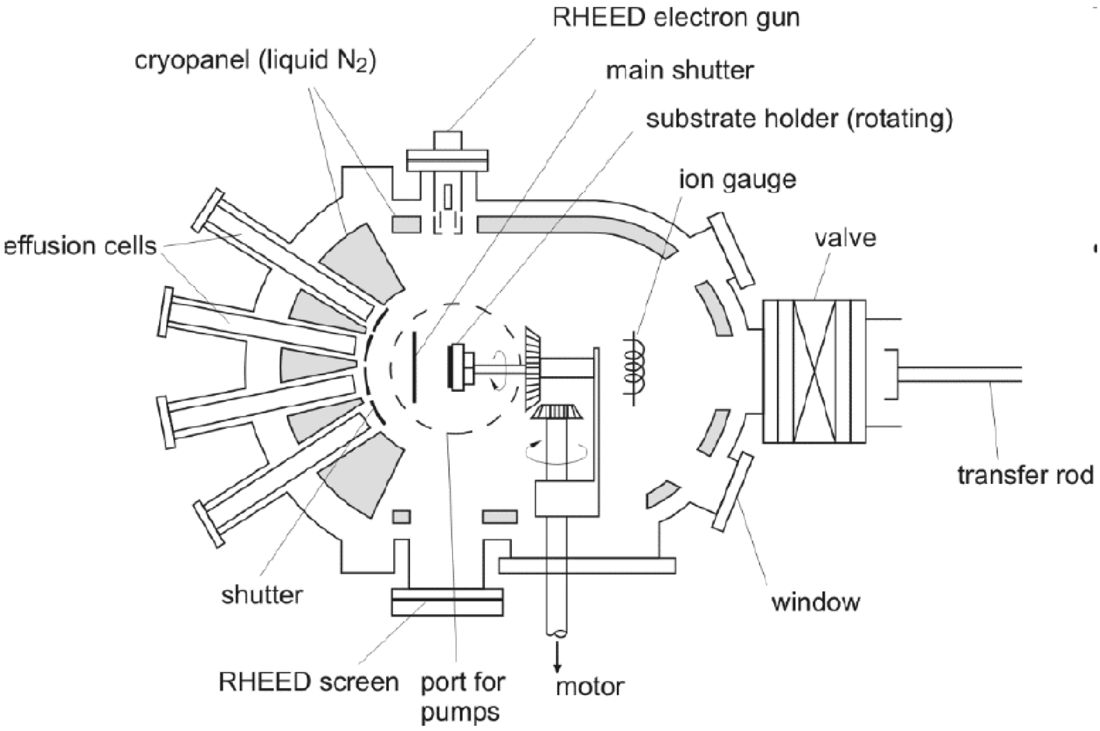


Figure 1.2: *A schematic of a typical MBE system and its components[16].*

Fig. 1.1 (b). The GaSb E_v lies about 160 meV above the InAs E_c. Such a configuration leads to transfer of carriers from the GaSb valence band to the InAs conduction band, resulting in a semi-metallic structure. This results in an ambipolar transport behavior, i.e., transport due to electrons in the InAs core as well as holes in the GaSb shell. An exact position of the potential barrier that exists between the two materials can only be estimated via simulations. This material system has been studied extensively in the layer systems due to the nearly strainless growth[7, 12, 10] and in the core/shell NWs configuration as well[13, 14].

1.2 Molecular Beam Epitaxy for SAE of InAs NWs

With recent efforts to achieve high purity, catalyst-free NWs, selective area epitaxy (SAE) using Molecular Beam Epitaxy (MBE) has been studied extensively. Catalyst-free growth is desirable to avoid contaminants (e.g., Au that gives deep level traps in the semiconductor) that are usually used to initiate the growth of the NW[15]. A combination of high purity source materials and Ultra High Vacuum (UHV) conditions (a pressure less than 1×10^{-9} Torr) within the MBE allows for growth of high-quality layers and NWs. Low growth rates of about 1 μm/h allow for better control of the thickness of the desired structures.

Fig. 1.2 shows a schematic representation of an MBE system[16]. The samples are placed on a rotatable substrate holder which rotates at 10 rpm during the growth run in order to obtain a uniform growth. Prior to transferring the sample into the growth chamber, it is heated to 700 °C for 45 min. The temperature of the cells dictates the amount of material that will be exposed to the substrate and shutters to each cell open and close the cells. The

MBE used in this work is a *Varian GenII* MBE equipped with an As- and an Sb- cracker cell, along with In and Ga effusion cells and Si and C doping cells. Ga and In deposition rates correspond to planar growth rates, whereas the As and Sb fluxes correspond to beam equivalent pressures (BEP) measured with an ion gauge at the position of the substrate.

Table 1.1 summarizes the temperature the cells are heated up to prior to the growth process. The As bulk reservoir temperature was in the range of 450 C° - 480 °C. This is done to have an improved and stable flux rate with decreasing amount of material. Afterward, the chamber was opened up to refill As and the bulk temperature was once again maintained at 450 °C. For a catalyst-free growth, two types of growth regimes are possible: Vapor-Liquid-Solid (VLS) where the group III element is the catalyst and a Vapor-Solid growth which does not require a catalyst[17, 18].

Element	Cell temperature (°C)
Ga Tip	1015
Ga	850
In Tip	970
In	820
As cracker	600
As bulk	450 - 480
Sb cracker	850
Sb bulk	635
Sb heater	800

Table 1.1: *Cell temperatures used for InAs and InAs/GaSb growth at the MBE in the Nanocluster.*

Following the growth conditions that were found to be favorable in [20] for a VS growth of InAs NWs on a Si(111) substrate based on the impact of growth parameters such as In rate and As flux, substrate temperature and growth time, the NWs in this work were grown similarly. The main point of difference is that in [20], the NWs were grown randomly whereas here, selective area epitaxy of NW arrays was carried out and optimized for InAs as well as InAs/GaSb core/shell NWs for more control over the position, size and directionality.

The growth mechanism of InAs NWs on Si(111) can be explained in a very brief and simplified manner in the following way. The NW growth is controlled by two mechanisms, namely, diffusion of the adatoms and direct incorporation of the impinging species. Direct impingement is not found to affect the growth much[20]. The substrate temperature controls the diffusion of the adatoms; increasing substrate temperature increases the diffusion of the adatoms, in turn reducing the sticking coefficient and vice versa. An optimum temperature window for optimum growth was determined as 480 °C-510 °C in [17] and a substrate temperature of 480 °C was used in this work. The NW growth starts with the impinging of atoms from the In and As sources into the growth chamber. In-rich areas on Si surface lead to nucleation of InAs in the holes obtained by diffusion. From this seed the NW starts to grow. This is one of the possible explanations for the NW growth and is schematically

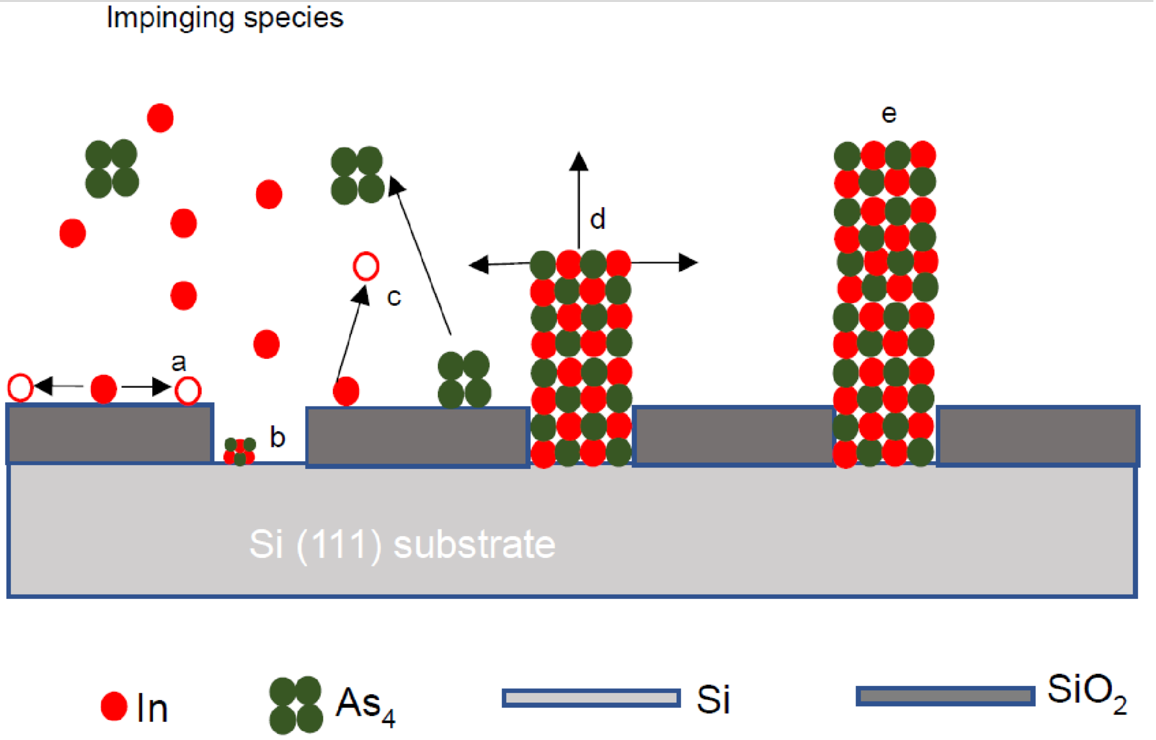


Figure 1.3: *Schematic representation of InAs NW growth. (a) Surface diffusion of In atoms, for confining into holes (b) formation of critical nuclei (c) Desorption of In and As from the oxide surface (d) NW starts to grow in radial and axial direction (e) vertical NW growth. Adapted from [19].*

depicted in Fig. 1.3 [19].

1.3 Critical thickness in semiconductor heterostructures

Due to a lattice mismatch between two different materials, combining them might result in a strained structure. Above a certain value, this strain relaxes by formation of dislocations [21]. This value corresponds to a critical thickness t_c, above which it is energetically more favorable to form a dislocation [21]. Below t_c, pseudo-morphic growth takes place with coherently strained layers, and above t_c, the strain is relaxed via a dislocation. This is schematically shown in Fig. 1.4.

A dislocation is a perfect dislocation if the Burgers vector is the same as the translation vector of the lattice. A partial dislocation is when the dislocation energy decreases, due to splitting of the perfect dislocation into partial ones. Thus, a stacking fault is created when partial dislocations modify the stacking sequence. To summarize, these partial dislocations are considered in terms of stacking faults created in the shell or the core depending on type of dislocation.

A core-shell NW model by Rayachaudhari and Yu[22] to predict the critical dimensions in core-shell NWs for ZB and WZ structures was implemented to calculate the t_c for the

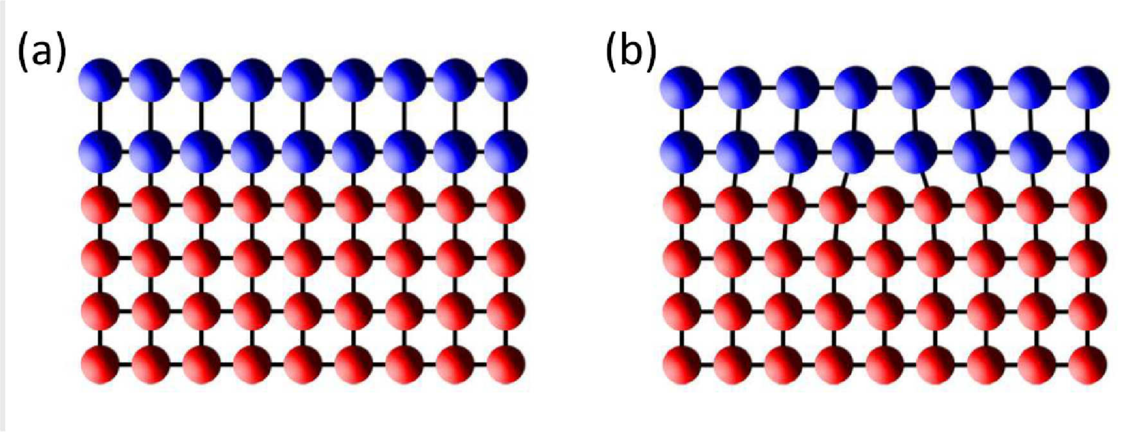


__Figure 1.4:__ Schematic representation of an epitaxial layer interface between materials with different lattice constants. (a) strain relaxed system and (b) relaxed by inclusion of a misfit dislocation. Adapted from [16].

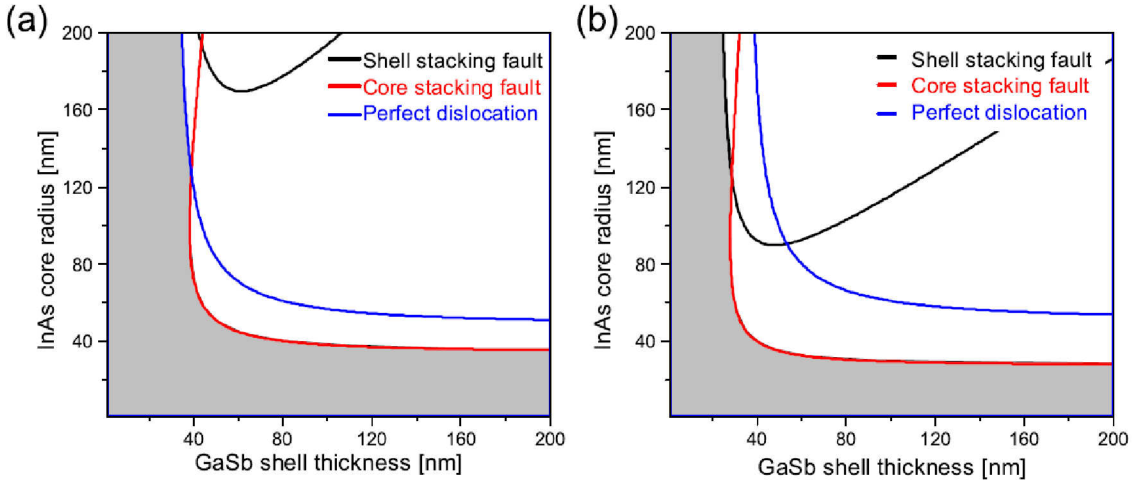


__Figure 1.5:__ Critical dimension maps of (a) ZB InAs/GaSb, (b) WZ InAs/GaSb. The black lines indicate the critical dimension for shell stacking faults, red line for core stacking faults and blue lines for perfect dislocations. The grey regions corresponding to misfit dislocation free structure. Taken from [20].

InAs/GaSb material system in the PhD thesis of Torsten Rieger[20]. The model assumes cylindrical NWs without any facets and is based on a comparison of the strain energy in the NW and the energy associated with dislocations. The elastic constants and lattice parameters are also not known and only obtained from theory. Due to the significantly lower lattice mismatch for InAs/GaSb, a higher t_c is expected. The calculations are presented in Fig. 1.5[20]. Theoretically, coherent growth is expected for a core radius below 40 nm or a shell thickness below 35 nm. Considering the critical dimensions defined by stacking faults in the core, no major difference between ZB and WZ core/shell NWs is observed.

Since, in this work, the growth parameters are optimized for an InAs core of 90-100 nm and a GaSb shell of thickness 20-25 nm, it is considered to be a misfit dislocation free system. Transmission Electron Microscopy (TEM) conducted on similarly processed NWs [19, 20] confirm these results. Fig. 1.6 displays a TEM image of the interface of the two

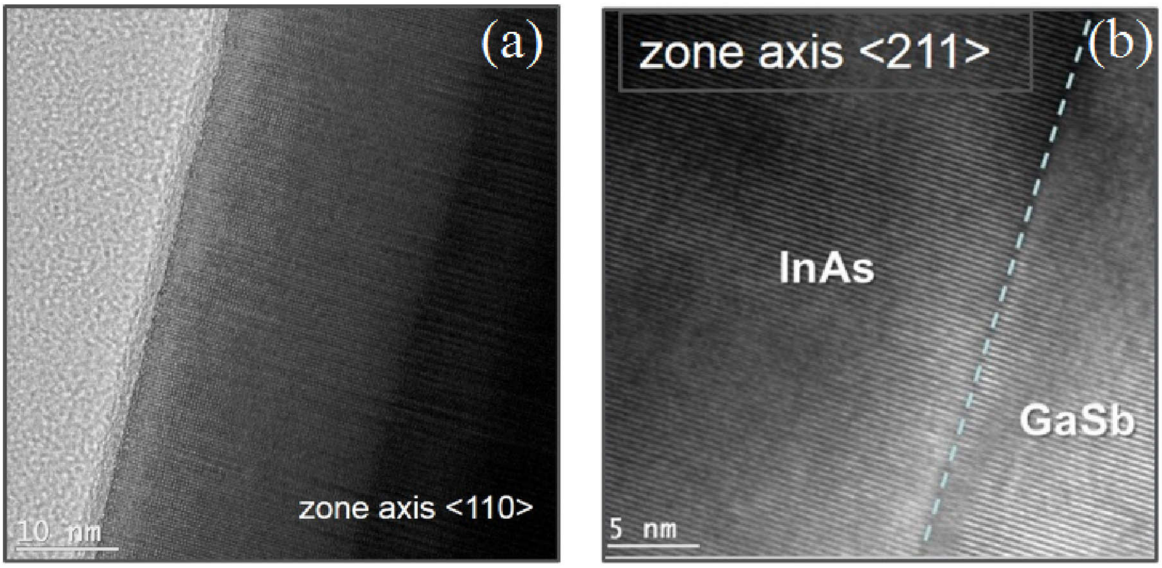


Figure 1.6: *(a) TEM image of stacking faults that are induced from the InAs core to the GaSb shell. (b) TEM image of the InAs/GaSb NW interface. Taken from [19]*

semiconductors without any misfit dislocations. Stacking faults and twinning faults however are translated from the core to the shell. This once again emphasizes that semiconductors with low lattice mismatch can be combined into core-shell NW geometry without any misfit dislocations.

1.4 Basics of field effect type measurements

Electronic transport on a macroscopic scale is governed by several factors and contributions, the most well-known of which is the Ohm's law. In the classical transport regime, the wave nature of the electron and the effective quantum phenomenon arising out of that is neglected. The impact of electron scattering for a sufficiently large system is averaged out and the charge transport is described by the drift velocity v_d. Expressions for current density j, resistivity ρ conductivity σ, mobility μ, etc. can be derived under these assumptions[16]. This is known as the Drude model. Although the Drude model does not consider the quantum mechanical nature of electrons, these expressions can be corrected if the effective mass of the electron or the hole m_{eff} is considered. This section considers the classical model and the corrections to low dimensional transport are discussed in the next section.

The NW device fabricated in this work can be compared to a Tunneling Field Effect Transistor (TFET). The NW is the conducting channel that is contacted by source and drain metal contacts (see Fig. 1.7). The NW is placed on a conductive substrate (Si(100)) covered with a dielectric (150 nm of SiO_2) which serves as a back-gate (BG).

Thus, parameters like resistance R, resistivity ρ, charge carrier concentration n, charge carrier mobility μ can be extracted from the IV characteristics ($I(V_{sd})$) as well as field effect transfer characteristics ($I(V_g)$). Fig. 1.8 shows similar measurements used to extract these

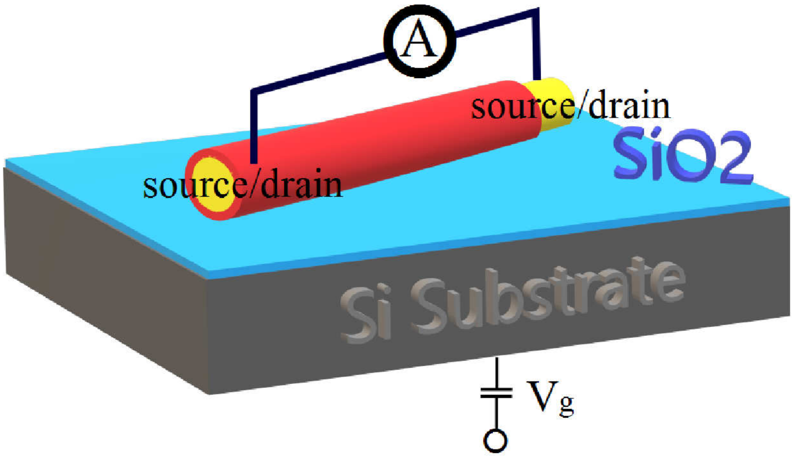


Figure 1.7: *Schematic of a NW used as a field-effect transistor where the SiO_2 substrate serves as a back-gate that is capacitively coupled to the NW by V_g. A voltage V_{sd} can be applied between the source and drain contacts and the resulting I_{sd} can be measured.*

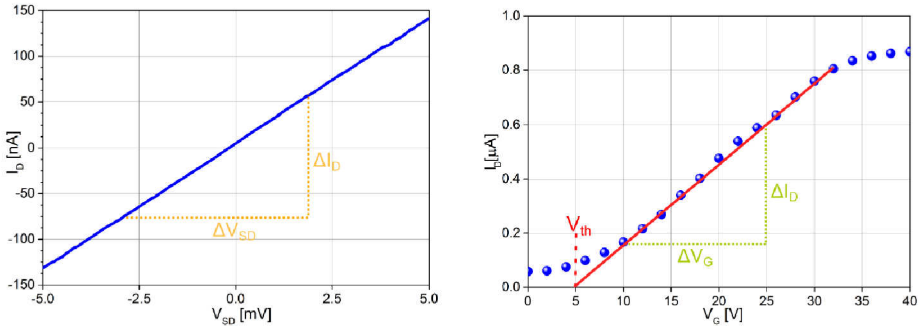


Figure 1.8: *Typical IV characteristics (left) and field-effect transfer characteristics (right). (a) V_{th} denotes the threshold voltage. The resistance can be extracted from the IV curve. (b) The trans-conductance g_m can be extracted from the field effect characteristics. Figure taken from[23].*

values in the following way[23]. R and ρ (considering the NW to be of hexagonal geometry and accordingly calculating the cross-section) can be calculated as:

$$R = G^{-1} = (\Delta I_{sd}/\Delta V_{sd})^{-1} \tag{1.1}$$

$$\rho = R \times A/l \tag{1.2}$$

where l is the length of the conducting channel and equivalent to the source and drain contact separation. µ and n need to be extracted from the field effect characteristics. In a field effect transistor and hence effectively in the NW, the conductance between the source and drain can be modified with an electric field. A gate electrode is usually capacitively coupled to the NW and depending on the polarity can cause accumulation or depletion of charge carriers by electrostatic induction. The response of the conductance can be qualitatively determined by calculating the slope of the IV characteristics, called trans-conductance:

$$g_m = dI/dV_g \tag{1.3}$$

The threshold voltage V_{th} is the gate voltage at which the transistor switches from non-conductive to conductive and is estimated by extrapolating the linear region of the IV curve and determining the x-intercept. This value of V_{th} can be understood as the voltage at which the conductance is negligible due to depletion of the charge carriers. In an ideal case, the charge carrier density at V_{th} is the intrinsic charge carrier density but reversed in polarity.

1.5 Low dimensional transport

The NWs studied in this work exhibit a diameter of 150 nm and a length up to 4 μm. Thus, the expressions governing the electrical transport derived from the Drude model might be inappropriate to be used at these length scales or at least require corrections. Also, in samples of high crystal quality, the electronic transport could be ballistic or even phase coherent. Thus to assess the transport confined to lower dimensions it is necessary to define characteristic length scales. The following sections follow from the lecture notes in[24] and briefly introduce the concepts required to follow the analysis of the magneto-transport measurements conducted in section 15.2.

1.5.1 Characteristic length scales

Mean free path
l_m, the mean free path, is the average distance an electron travels until it is scattered, i.e., before its momentum is altered due to scattering at defects, impurities or phonons. Since phonon scattering is suppressed for low temperatures, it increases until the impurity or defect scattering start contributing. Depending on whether this scattering is elastic or inelastic, momentum transfer or randomization of phase occurs respectively.

Phase coherence length
l_ϕ, the phase coherence length is a measure of the length electrons can travel before their phase is randomized. The phase is modified at every scattering event and the phase is shifted by the exact same amount if the electron would travel the same path a second time. This is in contrast to inelastic scattering events for e.g., with a phonon, where the phase shift acquired is different each time since the scattering mechanism is statistically in space and time. Electron interference occurs for length scales up to l_ϕ. This is also temperature dependent since scattering centers freeze out with lower temperatures.

Fermi wavelength
$\lambda_F = 2\pi/k_F$ is the Fermi wavelength is the wavelength associated to an electron at the Fermi edge with Fermi wave vector k_F. It can used to define the dimensionality of the system. A system with length L, width W and thickness t is:

- 3D if $L, W, t >> \lambda_F$

- 2D if $L, W >> \lambda_F, t << \lambda_F$ and
- 1D if $L >> \lambda_F, W, t << \lambda_F$

1.5.2 Transport regimes

Regarding charge transport, mesoscopic systems are of interest because of the occurrence of quantum interference phenomena like universal conductance fluctuations (UCFs). The different transport regimes can be classified by relating the system size L with other relevant length scales of charge transport described before.

$L << l_m$ defines a transport regime for which the scattering at the sample boundaries dominates and scattering inside the system can be neglected. This is known as the basllistic regime. $L >> l_m$ defines the diffusive regime where the scattering at defects, impurities etc. inside the sample dominates.

For $L << l_\phi$ mesoscopic transport occurs where the electrons are fully able to interfere and quantum interference phenomena can occur. For $L >> l_\phi$, the phase information averages out and the transport can be treated quasi-classical.

1.5.3 Quantum confinement and Conductance quantization

Quantum confinement

If one of the sample dimension is in the range of or smaller than λ_F this results in the transport being confined in that direction. This is known as quantum confinement and can be considered as a 3D electron gas which is confined by infinite potential barriers at $z = \pm L/2$ where L is the sample length. The corresponding energy eigenvalues are:

$$\epsilon_n = \frac{\hbar^2 k_{z,n}^2}{2m^*} = \frac{\hbar^2}{2m^*}\frac{\pi^2}{L^2}n^2 \tag{1.4}$$

Thus the dispersion relation for a free 3D electron gas changes to:

$$E_n = E_|| + \epsilon_n = \frac{\hbar^2 k_{||}^2}{2m^*} + \frac{\hbar^2}{2m^*}\frac{\pi^2}{L^2}n^2 \tag{1.5}$$

where $k_{||} = k_x^2 + k_y^2$. This is equivalent to the energy band splitting into sub-bands with energy ϵ_n for k=0. ϵ_1 is then the confinement energy also known as the ground state energy. Similarly, for a 1D system where this is confined now in two directions, the dispersion relation is given by:

$$E_{n_1,n_2} = \frac{\hbar^2 k_x^2}{2m^*} + \epsilon_{n_1,n_2} = \frac{\hbar^2 k_x^2}{2m^*} + \frac{\hbar^2}{2m^*}\frac{\pi^2}{L_y^2}n_1^2 + \frac{\hbar^2}{2m^*}\frac{\pi^2}{L_z^2}n_2^2 \tag{1.6}$$

Only the subbands that fall below the chemical potential are occupied and correspond to a transport channel for conductance to occur.

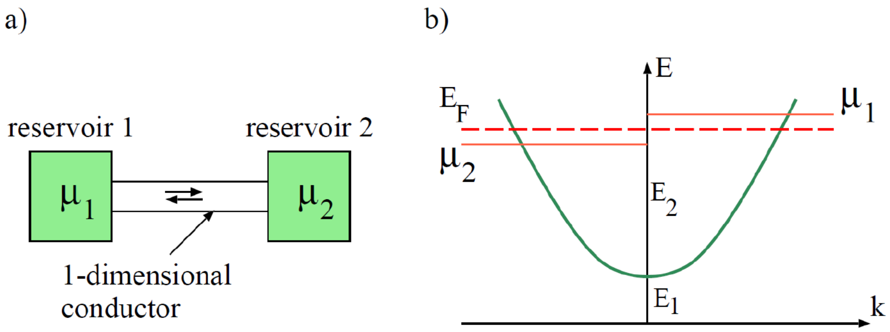


Figure 1.9: *Schematic depiction of a 1D conductor with length L width W between the two reservoirs with chemical potential μ_1 and μ_2. The potential difference caused by an external applied voltage results in the transfer of electrons for which the energy lies within the range of the chemical potentials, from one reservoir to the other. Adapted from[24].*

Conductance quantization

A very intuitive interpretation of the macroscopic resistance of a sample was given by Landauer and by Büttiker in their model as:

$$R_{mn,kl} = \frac{U_{kl}}{I_{nm}} \tag{1.7}$$

where the resistance is defined by the voltage measured between contacts k and l and the current flowing between n and m. If one restricts themselves to single channel transport with unity transmission probability, then the quantized conductance of a 1D conductor of length L and width W and area A where $W \approx \sqrt{A}$ can be directly derived using the Landau-Büttiker formalism [25]. The conductor is connected on the two sides to reservoirs with the electro-chemical potential μ_1 and μ_2, respectively, as shown in Fig. 1.9. The number of occupied channels within the conductor is denoted by N.

For $L << l_m$, due to ballistic transport a perfect transport between the reservoirs is expected as there are no scattering events. The potential difference $\Delta\mu = \mu_1 - \mu_2$ only drops at the contacts and not through the conducting channel. Under these assumptions, for electrons with wave vector k_l from contact 1 and with wave vector k_r from contact 2 have a quasi-potential μ_1 and μ_2 respectively. Following from the formalism, the current is given as:

$$I = \frac{2e}{W}(\sum \frac{\hbar(k_l - k_r)}{m*}). \tag{1.8}$$

Using the Fermi distribution function $f(E - \mu_{1,2})$, this reduces to

$$I = \frac{2e}{h}(\mu_1 - \mu_2) \tag{1.9}$$

Only electrons in the energy range between μ_1 and μ_2 contribute to the current. With an external applied voltage U, the equilibrium is disturbed and $\mu_1 = \mu_2 + eU$. The conductance for such a 1D ballistic transport with a factor of 2 to account for spin degenracy yields:

$$G_0 = \frac{2e^2}{h} \tag{1.10}$$

1.5.4 Universal conductance fluctuations

Universal Conductance Fluctuations (UCFs), explained theoretically by Altshuler *et al* and Lee and Stone[26, 27, 28], is the effect that leads to variations in conductance G of a sample in the order of e^2/h. UCFs can occurs in samples of dimension L which is around the same scale as the phase coherent length l_ϕ. They originate from the electron trajectories with the same start and end point in between which they gather arbitrary phases due to their diffusive motion. Lee and Stone showed that the interference term does not average out for sample dimensions smaller than l_ϕ. The fluctuations have a universal amplitude of e^2/h and they are a universal feature of quantum transport independent of the degree of disorder and sample size as long as $L << l_\phi$.

To observe them experimentally, a fluctuating conductance can be observed by a varying magnetic field B penetrating the sample area or by a variation of the Fermi energy E_f. It was shown that a sufficient change in E_f or B is equivalent to a complete change in impurity configuration, i.e., of the scattering centers. A change in the electron energy $\Delta E = E_c$ leads to a new conductance $G(E + E_c)$ which is statistically uncorrelated to $G(E)$. This should be equivalently observed for a variation caused by B.

For a detailed description of the calculation of the correlation field, average oscillation amplitudes and how these can help determine l_ϕ and other characteristic length scales, the articles by Beenakker and vHouten[29, 30] as well as the Ph.D. thesis of Christian Blömers[31] were used for reference. In the section 15.2, only the necessary definitions are described briefly to understand the nature of the analysis.

Selective Area Epitaxy of InAs/GaSb core/shell Nanowires

“The true delight is in the finding out rather than in the knowing.”

- Isaac Asimov

2 Introduction

Self-assisted growth of InAs NWs on Si substrates has been obtained with thin oxide layers and found to be reproducible[18]. In the Ph.D. thesis of Torsten Rieger[20], InAs as well as InAs/GaSb core/shell NWs were grown studying in detail the impact of growth parameters on the NW morphology, yield and crystal composition. In the Ph.D. thesis of Simon Hertenberger [32], position controlled growth of InAs NWs was studied extensively and the growth kinetics of the NW with respect to Selective Area Epitaxy (SAE) were discussed. Following these, the same is implemented towards position controlled growth of InAs/GaSb core/shell NWs. The catalyst-free SAE of InAs/GaSb core/shell NWs has been studied and optimized in the master thesis of Dinesh Arumugam[19]. While most of the parameters for the growth of these NWs remain the same for the scope of this work, certain changes were made to the process of substrate preparation such as the Electron Beam Lithography (EBL) design that defines the area for SAE and the Reactive Ion Etching (RIE) process parameters. The first part of this chapter briefly describes the already established process for SAE of the core/shell NWs and also discusses the changes incorporated for better results. The second part of the chapter describes the effect of the different RIE systems on the yield and dimensions of the NW. The change in the NW morphology due to substrate preparation, different growth conditions and doping concentrations are presented and analysed with the help of Scanning Electron Microscope (SEM) images. The effect of substrate temperature on the deposition of the GaSb shell on the InAs NWs is presented next. The last part of the chapter describes the elemental structure with EDX analysis of these NWs.

3 Substrate Preparation for SAE

The substrate preparation is a crucial step in SAE to have a good control over the vertical growth of the NWs. A high yield of vertical NWs, crystallite free growth as well as selectivity is desired for device based applications as well as to study quantum effects in these material systems. The effect of the In and As flux, growth time, dependence of the NW yield on the hole diameter and inter-wire distance (called pitch henceforth) following from [32] was found reproducible in[19] and the work of this thesis. Fig. 3.1 shows a schematic for the substrate preparation for SAE of the NWs[19].

- A 100 mm n-doped Si(111) wafer is first cleaned with the standard RCA cleaning as a service provided by the Helmholtz Nano Facility (HNF) cleanroom staff. This is to remove organic contaminants and oxide from the surface.
- The wafer is then oxidised using the Massoud model[33] for thermal oxidation at 990 °C for 30 min. These parameters are established for a SiO_2 thickness of 20 nm, which is later confirmed with ellipsometry.
- The wafer is then protective coated with AZ5214E resist at 4000 rpm for 30 s using the spin coater. This is done to protect the wafer surface from contamination caused during dicing of the sample. It is then diced into $2.5 \times 2.5\,\mathrm{cm}^2$ sized square samples.
- The samples are then cleaned to remove the AZ 5214 E resist in an ultrasonic bath with acetone and isopropyl alcohol (IPA) for 5 and 3 min respectively.
- The next step is to spin coat these samples with PMMA AR-P 679.04 950 K resist at 6000 rpm for 30 s and then soft bake it at 180 °C for 10 minutes. A 250 nm thick resist is obtained, which is confirmed with ellipsometry.
- The sample is then handed over for EBL writing to define the mask on the PMMA resist for SAE. After the writing process, the samples are developed in AR-600 55 developer for 70 s and the development is stopped by transferring the sample in an (IPA) bath for 3 minutes.
- An O_2 plasma cleaning for 15 s with 300 W and 200 sccm of O_2 flow is conducted after development to remove resist residues in the holes and thus obtain a cylindrical profile.
- Now, since the SiO_2 substrate is exposed in the areas that the resist was removed, the hole array pattern can be transferred onto it by a combination of dry and wet etching. The etching is not conducted solely with RIE to avoid damage to the Si surface (due

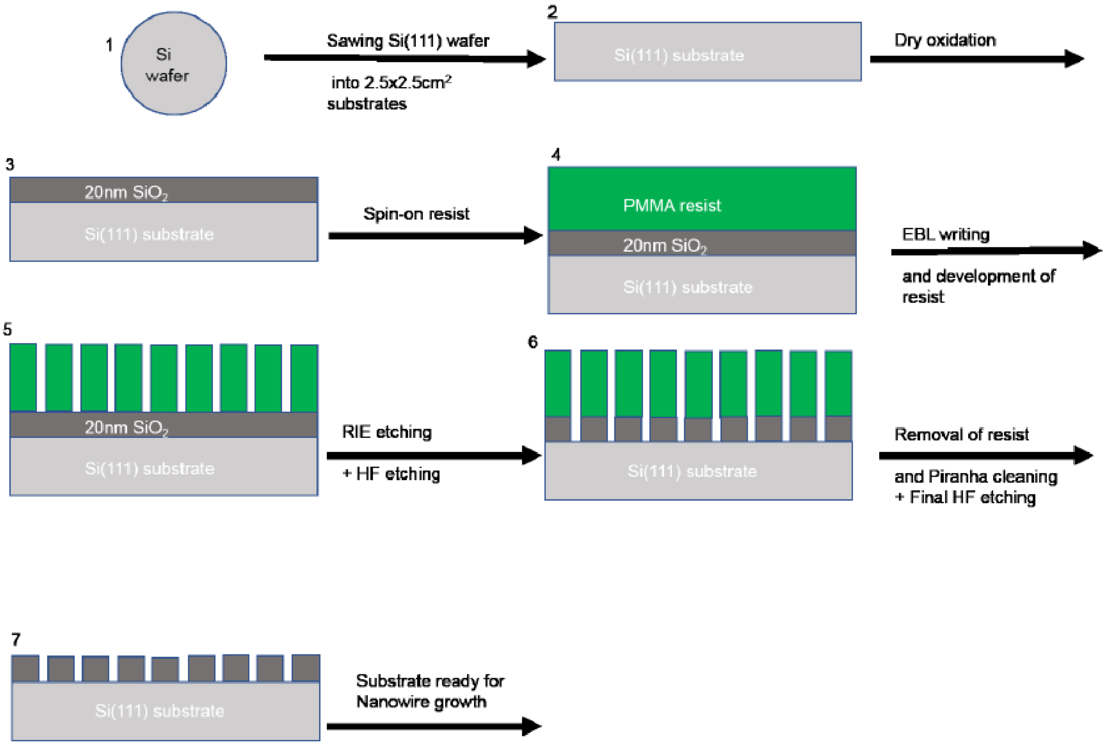


Figure 3.1: *Schematic of the steps involved in the fabrication of the Si(111) substrate for selective area growth of nanowires[19].*

to possible uncontrolled etching). The impact on NW growth and yield where a 20 nm oxide etched directly with RIE only and with a combination of RIE and wet etching has been presented in[19]. It was concluded that the use of a combination of both etching techniques reduces the chances of damaging the Si surface and thus increasing yield of the NWs. Thus, roughly 15 nm of the SiO_2 is removed first with RIE and the remaining 5 nm by dipping the sample in 1% HF for 60 s.

- After transfer of the pattern into the SiO_2 layer, the PMMA resist is removed using acetone and IPA. This is followed by a 15 minute O_2 plasma cleaning with a power of 300 W and 200 sccm gas flow rate.

- To remove any organic residues from the previous processing, the sample is cleaned in a piranha solution (H_2SO_4:H_2O_2 = 3:1; 96% H_2SO_4 and 37% H_2O_2) for 10 minutes. The sample is then rinsed in De-Ionised (DI) water.

- As a final step to remove native oxide from the Si surface, the sample is dipped for 60 s in 1% HF prior to loading into the MBE chamber for growth.

- The sample is then loaded into the MBE load lock as soon as possible to avoid regrowth of native oxide.

3.1 Optimization of RIE and EBL

Several AFM tests were conducted on these substrates to check the accuracy and reproducibility of these process parameters. Growth runs to grow InAs NWs were conducted on these samples and the results proved the need to re-consider certain parameters of substrate processing. This means that the NW yield was too low and incomparable to the results obtained in the work of[19]. Fig 3.2 displays samples with very low yield of NWs and samples with more crystallites than NWs. The highlighted parts of the Fig. 3.2 (e) show empty holes, implying incomplete etching of the SiO_2 and growth of a crystallite implying damage to the Si(111) surface. Fig. 3.2 (d) shows an overall gradient in the growth of the NWs indicating uneven etching of the SiO_2. This implied that the problem was due to incomplete and uneven etching of the SiO_2.

Thus, changes to this process had to be made to account for the process parameters that were found to be irreproducible. These were the RIE parameters and the EBL mask. The etch rates from RIE were determined again using test samples with SiO_2. Ellipsometry measurements were conducted on such samples before and after RIE to determine the oxide thickness and thus to obtain an average etch rate. A possible explanation for this discrepancy in the etch rates can be attributed to the multiple times that maintenance work was conducted on the RIE chamber dedicated to III-V materials (RIE-5) and also replacements of various parts. Due to frequent unavailability of this machine, the process was temporarily shifted to another RIE (RIE-4) which differed in chamber geometry. A comparative study of the etch rates obtained in both the systems in showed in Fig. 3.3.

The mask used to define the arrays for SAE had multiple fields with a range of varying hole diameter, pitch (distance between consecutive holes) and EBL doses. However, this was only used for the first few NW growth tests. A new mask (see Fig. 3.5) was used for the growth during this work which was written on the samples with optimized EBL parameters (from[19]), and only consisting of 60 nm and 80 nm holes with a 4 μm pitch. The choice for these parameters was due to the fact that in [32, 19] it was deduced that the highest yield was obtained for a diameter greater than 40 nm and a pitch greater than 2 μm. The reason for this is attributed to growth regime dominated by diffusion limited rather than material competitive[32, 19]. Furthermore, Atomic Force Microscopy (AFM) was conducted on these samples to check the depth profile of the holes. These results are displayed in Fig. 3.4. These results also proved that the depth profile of the holes is more homogenous for a diameter of 60 nm and 80 nm.

The second modification made to the EBL design was with respect to the shape of the holes. The EBL writing of the array design on individual samples is a 14 h long process and to reduce this time, the mask was further modified to have a hexagonal hole pattern instead of a circular one (see Fig. 3.5). The writing time for the new design was reduced to under 2 hours and no change was observed in the growth of the NWs. This can be briefly explained in the following way. A circular hole was being defined by directing the electron

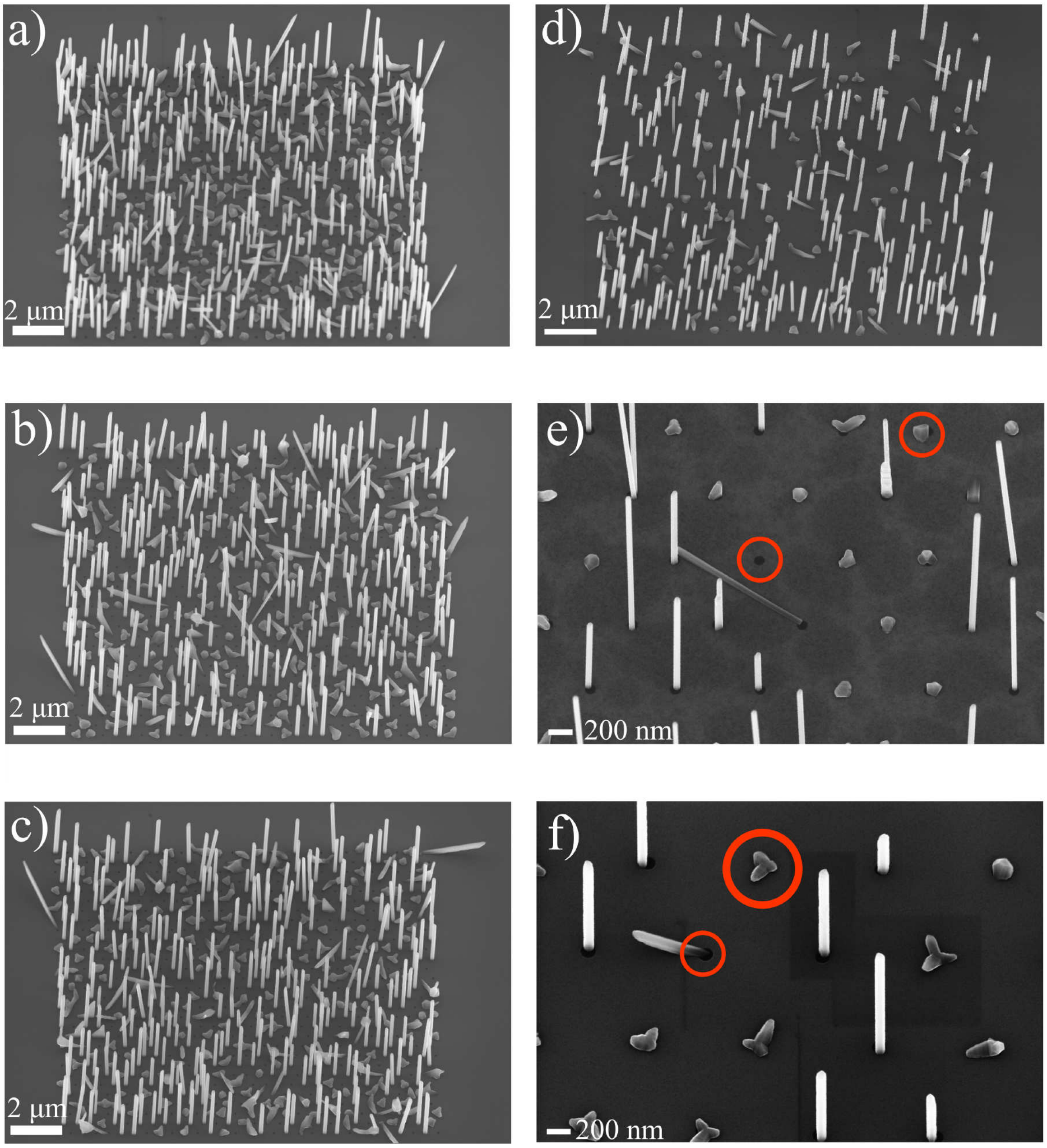


Figure 3.2: *(a), (b) and (c) display array of InAs NWs processed with pre-established parameters for RIE. (d) is an example of non-homogeneous etching of the* SiO_2*. (e) close-up of under-etched holes resulting in no NW growth and over-etched holes possibly resulting in crystallite formation. (f) close-up of crystallites and non-vertical NW growth due to damage to the Si(111) surface during etching*

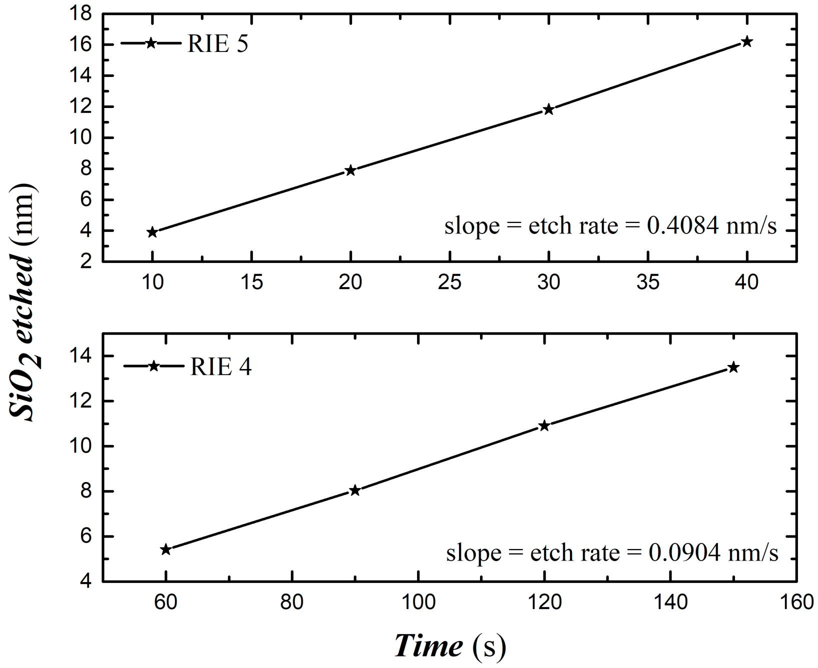


Figure 3.3: *A comparison of etch rates for different RIE machines used, inset shows the determined etch rate*

beam in a spiral which translates to definition of new co-ordinates for every 'point', however, a hexagonal shape was being defined by directing the electron beam in rows of 'points' and would result in fewer co-ordinates required and thus less time. InAs NWs were grown on a substrate with hexagonal holes and SEM pictures of this sample is compared with a sample with InAs NWs on a circular hole in Fig. 3.6. As can be seen, no change is observed in the NW morphology indicating that the hexagonal hole provides the same environment for facilitating the growth of the NWs as the perfectly circular one.

After incorporating the changes in the RIE and the EBL mask in the pre-established process, the results from the InAs NWs growth runs are displayed in Fig. 3.7. A top view of the image shows that most of the NWs are vertical along with a few tilted NWs and a few crystallites. The inset shows a close-up of the same sample with InAs NWs that are 4 μm apart. Thus, SAE of InAs NWs was successfully presented in this section. The paramaters used after optimisation are displayed in table 10.1

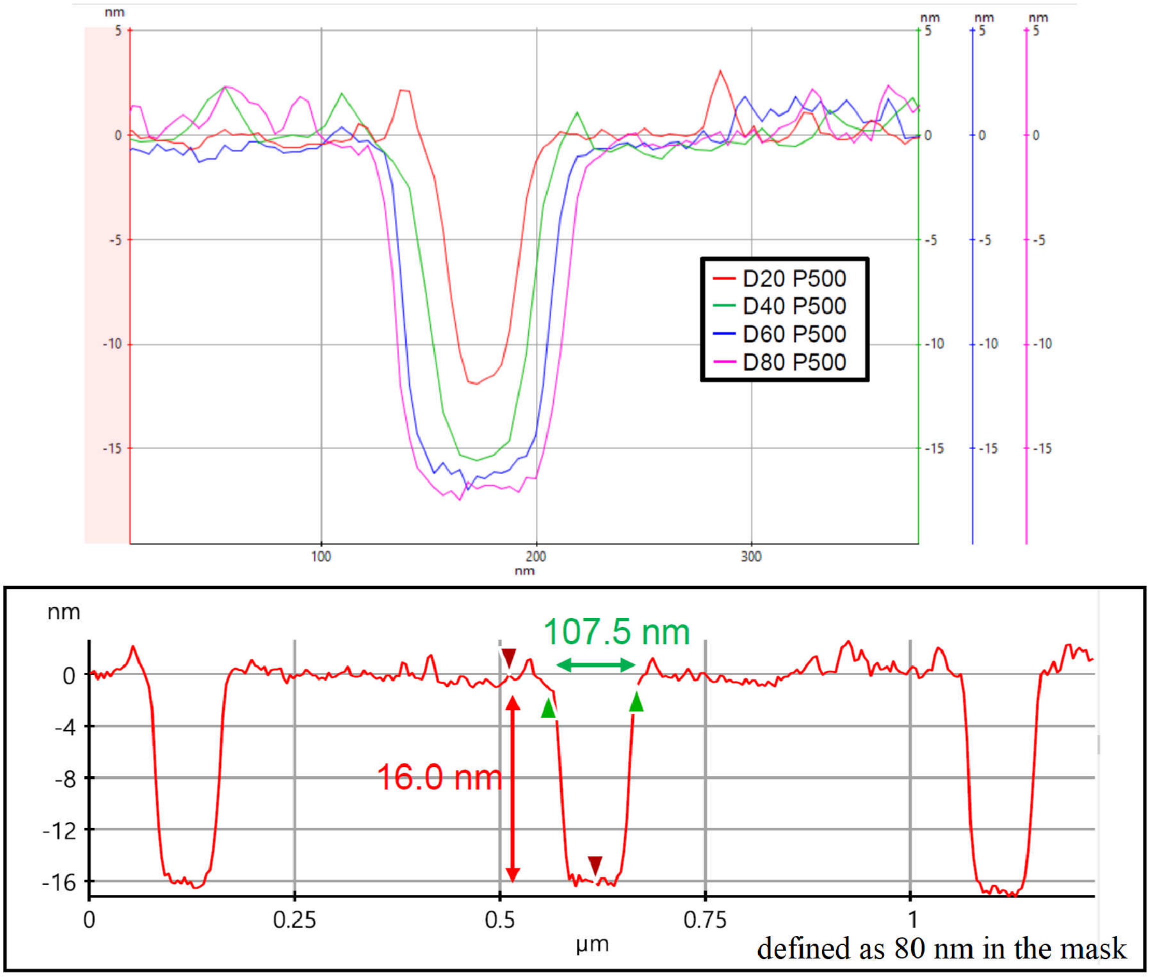


Figure 3.4: *A comparison of the depth and width profiles for diameters ranging from 20 nm until 80 nm and a pitch of 500 nm using AFM. The bottom scan shows a homogeneous depth and width profile for 3 consecutive holes of 80 nm diameter on a sample processed after optimization of RIE and EBL parameters.*

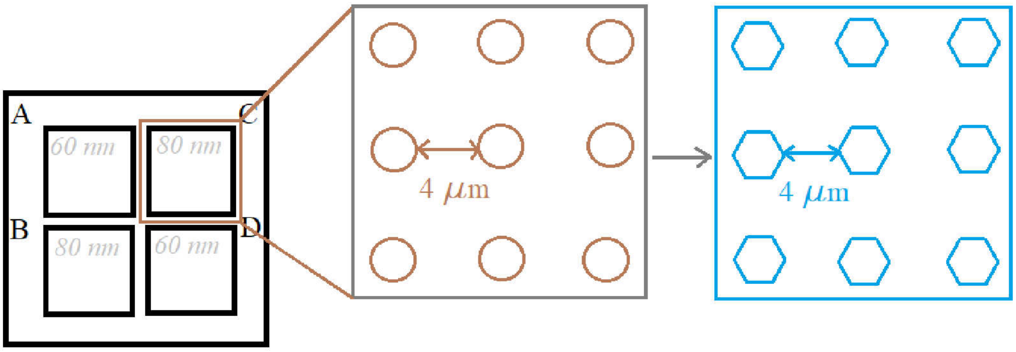


Figure 3.5: *Schematic of a substrate processed to have 4 fields with holes of diameters of 60 nm and 80 nm as labeled. First the holes were defined to be circular and later modified to a hexagonal shape to reduce writing time with EBL.*

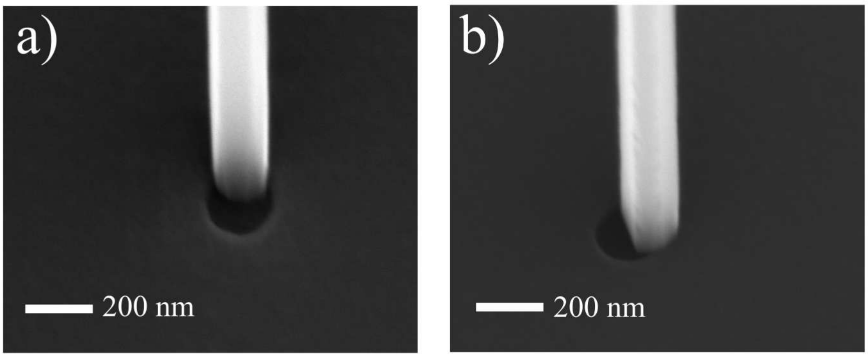


Figure 3.6: *(a) InAs NW grown out of a hexagonal shaped hole, b) InAs NW grown out of a circular shaped hole. No difference in the NW growth is observed with this change in the EBL design*

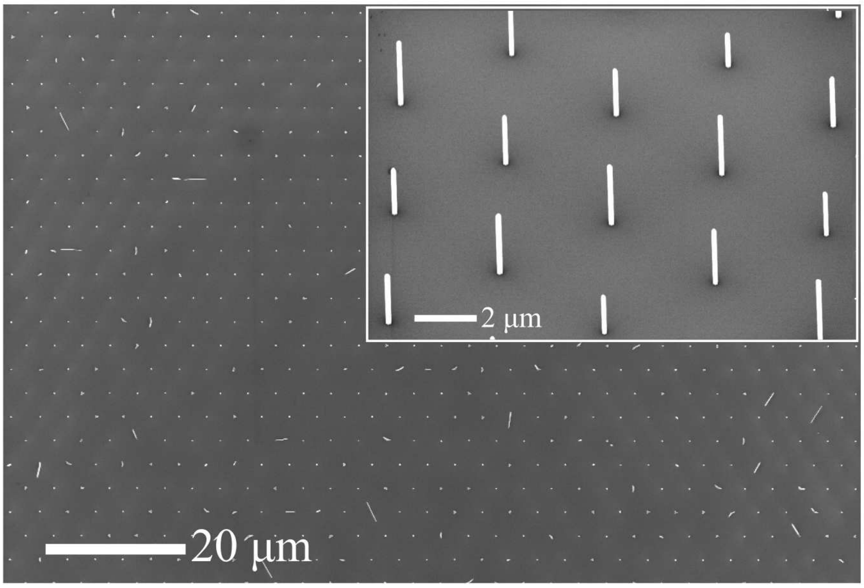


Figure 3.7: *A top view SEM image of InAs NW array showing high yield for vertical NWs. The inset shows a 30° tilted view of homogeneously grown InAs NWs with the newly optimized process for SAE. After incorporating the tilt, the NWs on average are approximately 3 µm long.*

4 MBE growth of InAs and InAs/GaSb core/shell NWs

With the optimization of the parameters for the substrate for SAE, the samples were first used for testing the growth of InAs NWs. After verifying the effectiveness and reproducibility of the growth process with respect to substrate preparation, the InAs/GaSb core/shell NWs were grown. The yield and morphology of the NWs depends on several factors such as the III/V ratio, substrate temperature, growth time, etc[20]. The following sections describe the effect of the In and As flux on the NW diameter, GaSb shell deposition, effect of C-doping of the GaSb shell on the NW morphology, and finally the effect of varying substrate temperatures during GaSb deposition.

4.1 Effect of In and As flux

Following the growth model of InAs NWs from section 1.2, the effects of the In rate and the As flux were studied in[19]. The starting values for these fluxes used were: an In rate of $0.08\,\mu\mathrm{m/h}$ and an As flux of 4×10^{-5} mbar. The substrate temperature for the growth of InAs NWs was 480 °C. These values were optimized in[19] with respect to high NW yield, low crystallite density and to obtain an average diameter of 150 nm. Fig. 4.1 (a) shows the sample with NWs that were grown with these conditions for a standard growth time of 2 h. The inset shows a NW with a diameter of 138 nm. NWs with a diameter less than 100 nm are desired for facilitating successful deposition of metallic contacts on the NWs for device fabrication. Also, the field applied with a gate voltage over the NW is inversely proportional to the square of the distance between the dielectric and the carriers that one wants to control within the NW. For probing quantum mechanical effects as well, a reduced diameter would facilitate lowering of classical contributions to the transport. Thus, in order to obtain this, a technique where the In rate and As flux is high at the beginning to facilitate nucleation, and are later reduced to only obtain axial growth[19] was tested.

Fig. 4.1 (b) shows a sample with NWs that were grown on similarly processed substrates for 2 h but with a reduced In rate of $0.08\,\mu\mathrm{m/h}$ and As flux of 2.5×10^{-5} mbar. The inset shows a NW with a diameter of 84 nm. It can also be seen that this technique still results in a high NW yield and a low crystallite density. The NWs were found to be, on average, of a homogenous length and diameter too. The average length obtained for a growth time of 2 h was found to be at least $4\,\mu\mathrm{m}$. Thus, henceforth, this technique was implemented for growth of InAs NWs to have a diameter smaller than 100 nm. Fig. 4.2 shows another sample with

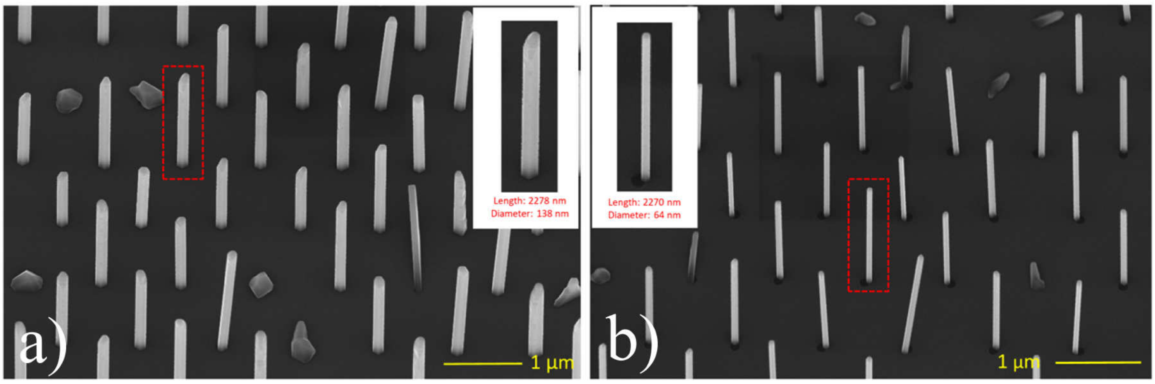


Figure 4.1: *SEM image at a 30° tilted view of an array of 80 nm diameter and 1 μm pitch on similarly processed substrates; inset shows close up of a single NW for comparison of the effect of reduced In and As fluxes during MBE growth on the NW diameter*

the same growth time, In rate and As flux to conclude that the substrate preparation was indeed optimized for position controlled vertical growth of InAs NWs and that the average length and diameter of the NW are also reproducible for the same parameters.

The reproducibility of this process can be observed in Fig. 4.2. NWs with diameter of 90 nm and length 4 μm are grown with high yield. From[20], it is known that these NWs show a hexagonal morphology with side facets of 110 type. The origin of the gradient at the very top of the NW is however unclear.

4.2 GaSb shell deposition

In this section, the growth parameters and growth kinetics during GaSb shell deposition are discussed. Since the MBE system which was in use during the work of[20, 19]and this work is the same, the pre-established parameters were used for reference. The Ga and Sb flux rates, growth time and the sequence of initiating shell growth on InAs NWs were kept the same and only the substrate temperature during shell deposition was tested out (discussed in section 4.4).

After the growth of InAs NWs as described in section 1.2, the sample is ready for GaSb shell deposition. The same module is also equipped with a Ga and Sb source, thus, after growing InAs NWs for 2 hours, the sample was cooled from 460 °C that is the growth temperature used for InAs NWs to 330 °C. The GaSb shell was grown with a Ga growth rate of 0.1 μm and Sb flux of 1.5×10^{-6} mbar. The shutter sequence was started with providing Sb for 2 min first and then Ga and Sb together with the aforementioned growth and flux rates respectively for 45 min. With a linear dependence of the shell thickness with respect to deposition time, this amount of time corresponds to a GaSb shell thickness of 25 nm[19]. This was later confirmed with estimations made with Energy Dispersive X-ray (EDX) measurements, discussed in section 5.1.

The substrate temperature was lowered for the GaSb shell deposition because a low sub-

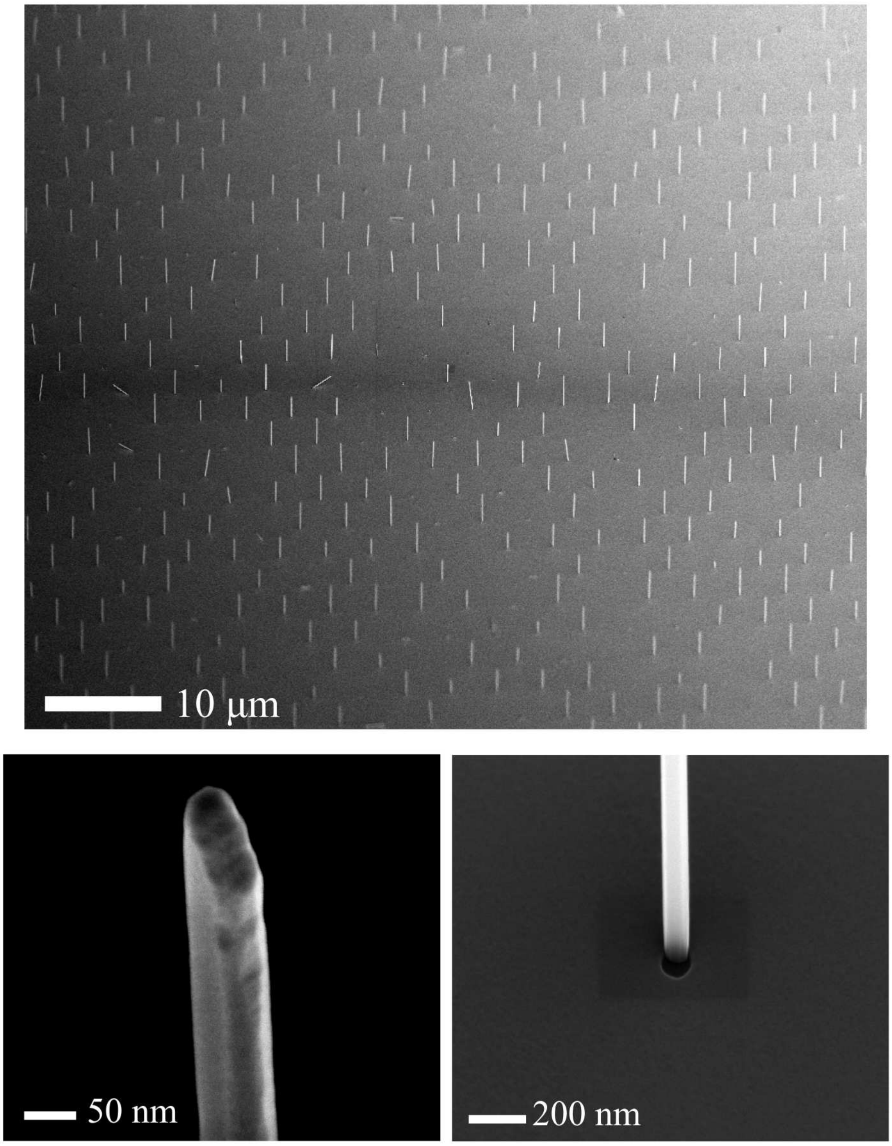


Figure 4.2: *SEM image at a 45° tilted view of an array of 80 nm diameter and 1 µm pitch. The InAs NW yield is high with very low crystallite density. The images at the bottom show a close-up of a single NW. The bottom of the NW shows a clear hexagonal morphology with side facets of 110 type[20]. The top of the NW shows a gradient with reducing facet size and hence a reducing diameter.*

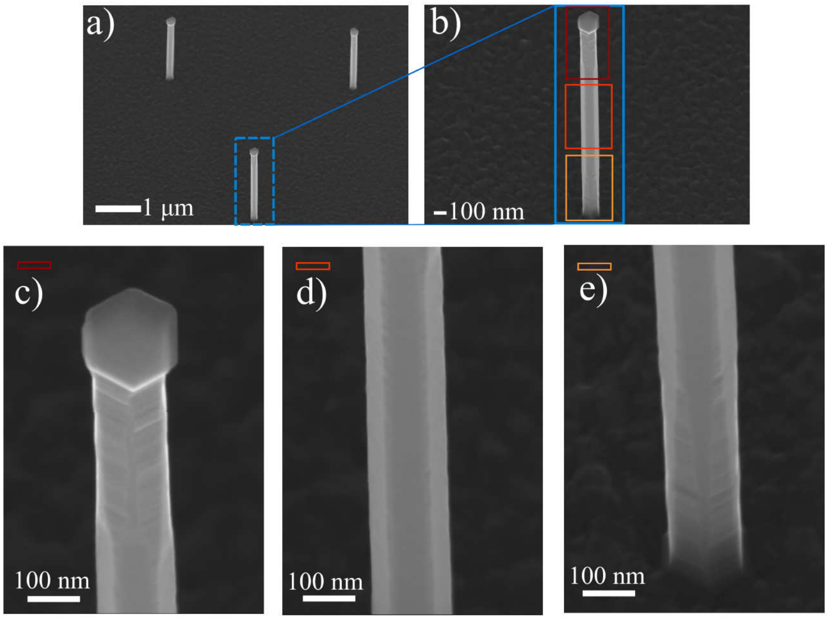


Figure 4.3: *(a) Array of InAs/GaSb core/shell NWs, (b) close-up of a single NW, (c) top of the NW with the GaSb platform, (d) middle of the NW showing tilt of the facets, (e) bottom of the NW*

strate temperature leads to reduced adatom mobility and enhanced sticking coefficient. As described later in section 4.4, a temperature of 330 °C was found to be ideal for a uniform coverage of the InAs NW with a GaSb shell. Since the NW density is low (1 NW/ 4 μm^2), shadowing effects for shell deposition due to neighbouring NWs, and the competition for the adatoms between neighbouring NWs are negligible. The start of the growth with a 2 min Sb-exposure is to create an InSb-like surface onto the InAs NW[20] and this time is also provided to rid the chamber of excess As.

Fig. 4.3 (a) displays one such sample with InAs/GaSb core/shell NWs with homogenous density and low density of crystallites. It also shows the GaSb parasitic growth onto the Si(111) substrate which is caused due to low diffusion and high sticking coefficient of the adatoms at this lower substrate temperature. Fig. 4.3 (b) shows a single NW and (c), (d) and (e) show more magnified images of the highlighted sections of this NW. The middle of the NW seems to have a similar morphology whereas a gradual shift of the facets is observed in the top and bottom 300 nm of the NW. This was already observed and analysed using HAADF profiles of the NW in[20]where the InAs NW core with six side facets of110 type was surrounded by a GaSb shell with a dodecagonal outer shape being bound by 110 and 211. This is presented in Fig. 4.4. This change in the cross-sectional shape along the NW axis was attributed to similar chemical potentials for adatoms at the GaSb 110 and 211 facets. This was also observed up to the longest shell growth time of 90 min. However, in order to investigate the origin of such behavior, the length of the InAs core and hence the InAs/GaSb core/shell NW could be varied from very short to very long. This will provide insight on whether the GaSb growth has a major contribution from direct impingement of

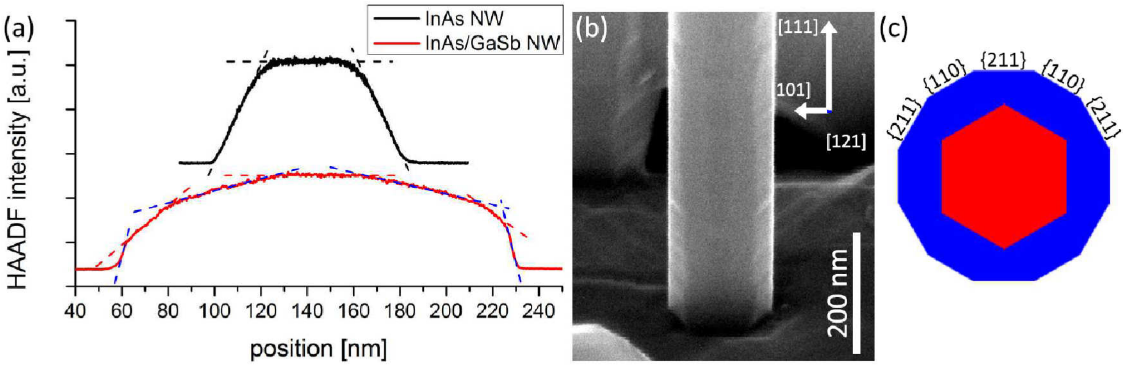


Figure 4.4: *HAADF profiles of InAs and InAs/GaSb core-shell NWs taken from the <110> zone axis. The profiles indicate the cross-sectional shape of the NWs. InAs NWs are bound by six 110 side facets while InAs/GaSb core-shell NWs are bound by twelve side facets belonging to the 110 and 211 family. Dashed lines are guides to the eye. (b) SEM image of the lower part of a core-shell NW showing the presence of multiple side facets. (c) Schematic of the cross-section of InAs/GaSb core-shell NWs[34].*

adatoms or via diffusion to or from the substrate. It will also indicate if there is a contribution from a possible temperature gradient along the NW. In addition to this, the formation of the hexagonal GaSb platform on top of the NW is also described in detail with the help of extensive TEM analysis in the PhD thesis of Torsten Rieger[20].

4.3 Doping of the GaSb shell

In this section the effect of various concentrations of Carbon to dope (C-dope) the GaSb p-type is discussed. Various C-doping concentrations were tested out during the GaSb shell growth. This was performed in the range of $6.25 \times 10^{18}/\text{cm}^3$ up to $5 \times 10^{19}/\text{cm}^3$. These concentrations correspond to the intended doping of GaAs layers in this MBE system. This was done to determine how the NW morphology and carrier concentration is affected in the NW. However, not all devices were measured during the scope of this work to be able to compare transport characteristics with varying doping concentrations.

Changes with respect to morphology of the NW are presented in Fig. 4.5. A general decrease in the size of the GaSb platform is observed with increasing doping concentrations. For the highest doping concentration of 5×10^{19} $/\text{cm}^3$, a slight shift in the hexagonal alignment of the NW is observed near the top. The highest doping concentration also shows multiple types of morphology especially at the top of the NW. Thus, without more crystal-structure analysis on these NWs, not much can be said about the effect of the doping concentrations but only that it definitely affects the preferential growth direction for the adatoms. The GaSb shell coverage is however still uniform and the EDX results show that the shell is of uniform thickness for all the doping concentrations. To further investigate the effects of C-doping, TEM could be performed on these NWs to determine the crystal structure along the NW and the InAs/GaSb interface. Gate dependent measurements could also be performed to compare the carrier concentrations obtained for each doping concentration.

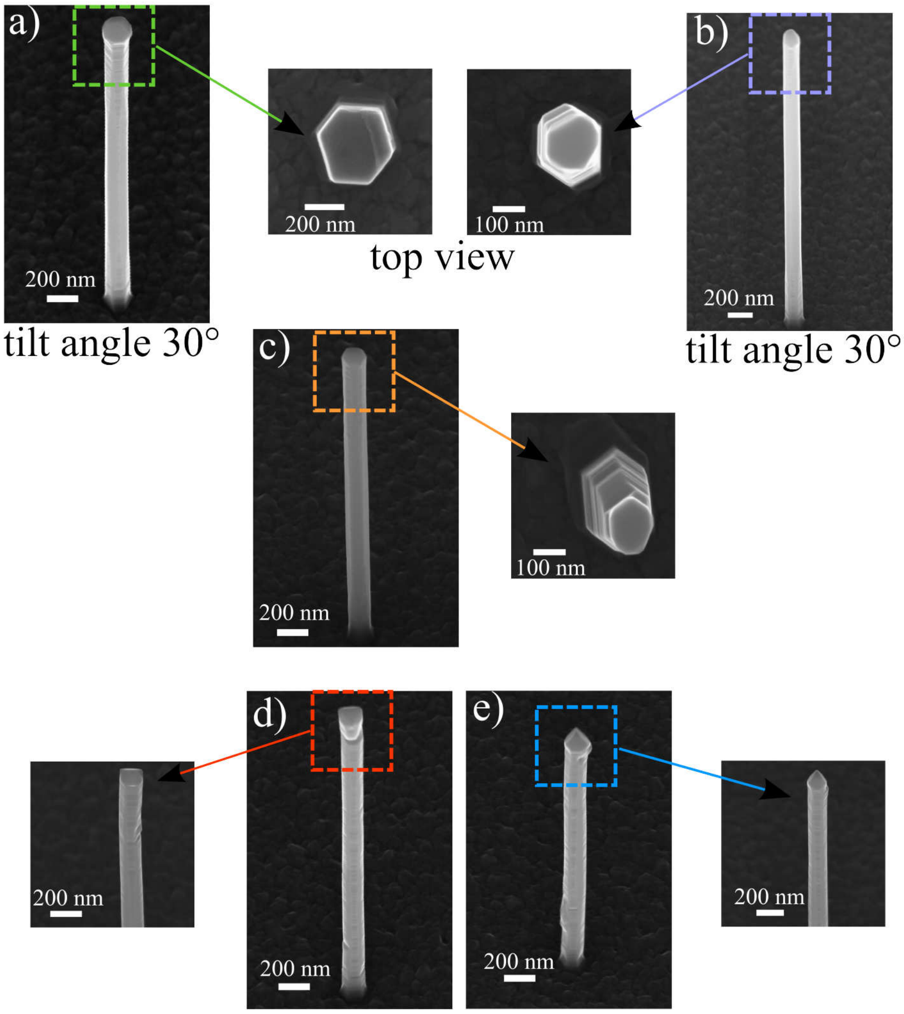


Figure 4.5: *InAs/GaSb core/shell NWs with different C-coping concentrations of the GaSb shell. (a) 6.25 × 10^{18} /cm^3, (b) 1.25 × 10^{19} /cm^3, (c) 2.5 × 10^{19} /cm^3, (d) and (e) 5 × 10^{19} /cm^3 with corresponding close-ups of the top of the NW. The GaSb platform is seen to be gradually decreasing with increasing doping concentrations. For the highest doping in (d) and (e), two different kinds of platforms are observed.*

4.4 Substrate temperature during GaSb shell deposition

Substrate temperature plays an important role during GaSb shell deposition since it controls the adatom mobility and its sticking coefficient. From[20], it was known that higher substrate temperatures lead to non-uniform shell deposition. With higher temperatures, an increasing inverse tapering in the morphology was observed. This non-uniformity however, would be advantageous to process devices which would allow access to the InAs core and the GaSb shell of the NW without requiring selective etching process for the GaSb shell. Thus, this was probed simultaneously with attempts to selectively etch part of the NW (described in section 8) to achieve the same.

Fig. 4.6 displays SEM images of NWs grown at temperatures higher than 330 °C (the optimized temperature for uniform GaSb shell deposition). As can be observed, with increasing temperatures an inverse tapering was observed. However, additional to this, a parasitic formation of a pedestal like structure was observed at the base of the NW. At the top of the NW a very uniform and much thicker ($\approx$ 100 nm thick) GaSb shell was also observed. A temperature gradient along the length of the NW, different facets at the top and bottom of the NW could be the possible explanation why the adatoms diffuse along the NW and settle at the top and bottom, leaving a $\approx$100 nm long section of the NW (more towards the base) without any material. The reason for uniform growth around the top and a highly non-uniform and yet crystalline growth at the bottom is unclear. This was also not observed in[20], however, the NWs there were not grown selectively.

For the highest two temperatures in the range, most of the NWs were observed to be horizontal rather than vertical. The morphological peculiarities observed with the SEM pictures, however, suggest that they might have fallen down after growth. This could be attributed to the parasitic growth at the bottom favoring to grow on the Si(111) substrate and forcing the NW to fall down. A gradually increasing surface roughness is also observed on the overall substrate with increasing temperature.

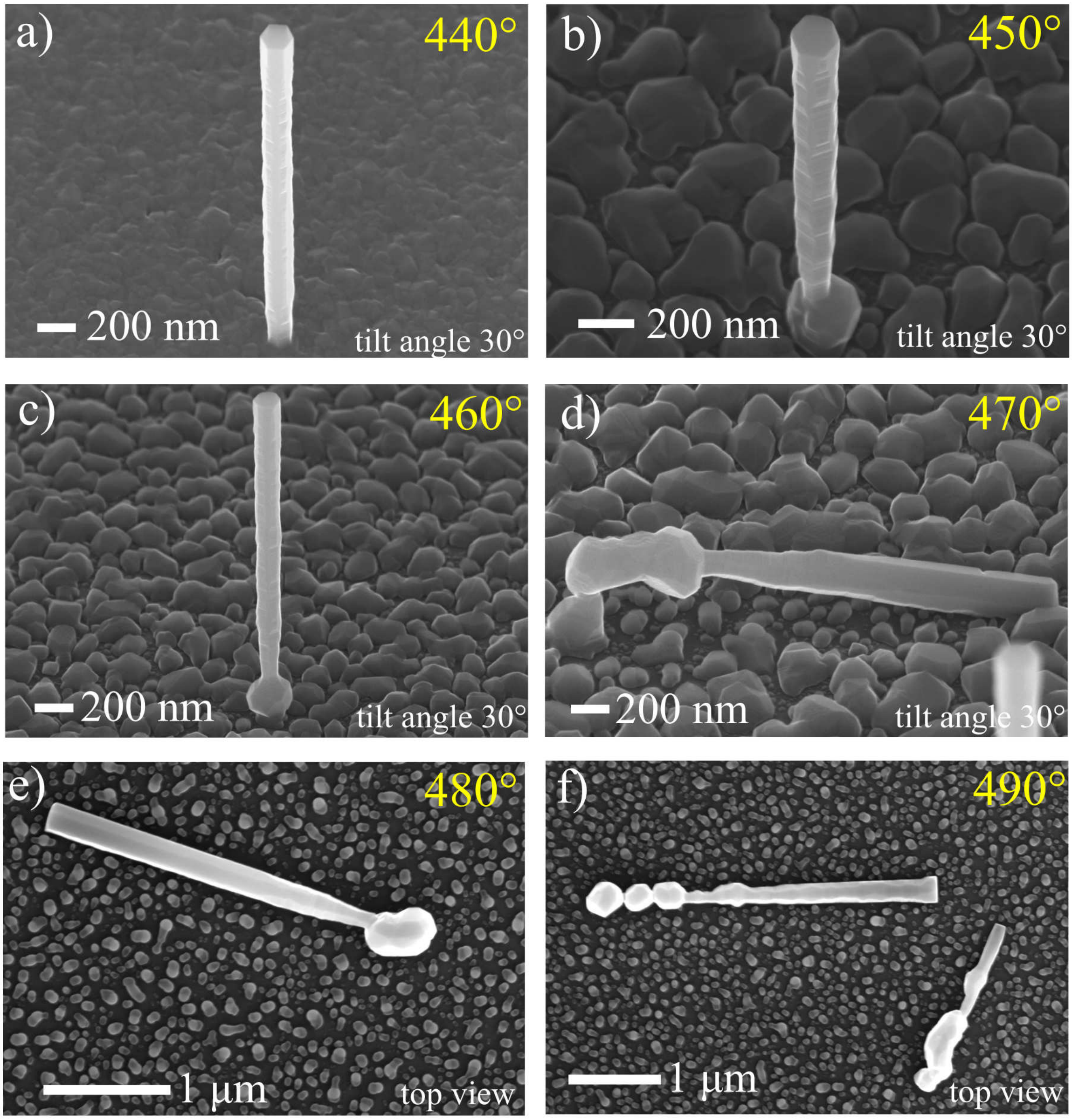


Figure 4.6: *(a) to (f) with increasing substrate temperatures during GaSb shell deposition. (a) to (c) still show vertical NWs and (d) to (f) show horizontal NWs, probably fallen down during growth.*

5 Elemental analysis on InAs/GaSb core/shell NWs

5.1 Energy Dispersive X-ray (EDX)

Energy Dispersive X-Ray measurements were conducted on the core/shell NWs from Fig. 4.6 (c) to check the elemental composition of the NWs. The substrate temperature during the shell deposition was 460 °C and as discussed in section 4.4, a parasitic growth at the bottom of the NW was observed. The shell thickness as observed from the SEM pictures is uneven throughout the NW and shows an inverse tapering. Several scans on different parts of the NW are showed in Fig. 5.1, Fig. 5.2, Fig. 5.3. The x-axis displays the segment scanned of the NW and the y-axis displays the relative magnitude of the corresponding elemental composition.

Fig. 5.1 (a) shows the top of the NW that was scanned. The corresponding scan shows high levels of Ga and Sb throughtout the scan with a slight decrease in the middle, where the core is present. As expected In and As show an increase in the middle of the area scanned that is the InAs core. In Fig. 5.1 (b), the scan is conducted at the thinnest part of the NW. Since the diameter of the core is not expected to change after shell deposition, and on comparison with the diameter determined for this part of the NW from the SEM image, it is concluded that the shell does not exist there or if it does, then only of a very small thickness. The scan shows high levels of In and As corresponding to the core and a comparable amount of Ga and Sb with a decrease near the core. This means a slight GaSb shell is indeed present there.

Fig. 5.2 (a) shows a scan conducted at the pedestal like parasitic formation at the bottom of the NW. The width of this structure is around 300 nm. The levels of Ga and Sb are much higher compared to the top of the NW from Fig. 5.1 (a). The In and As show a similar trend near the center of the NW again indicating the core being surrounded by GaSb. The Fig. 5.2 (b) shows the very bottom of the NW which was possible still inside the hole in the SiO_2 and thus probably wasn't exposed to the Ga and Sb impinging adatoms.

Fig. 5.3 shows a scan along the entire length of the NW and summarizes the information obtained from the previous scans separately conducted at the different part of the NW. EDX results are not very conclusive about the actual composition of the NW in these regions except that the individual elements are present in low or high amounts with respect to each other. In order to find out more about this influence of the substrate temperature

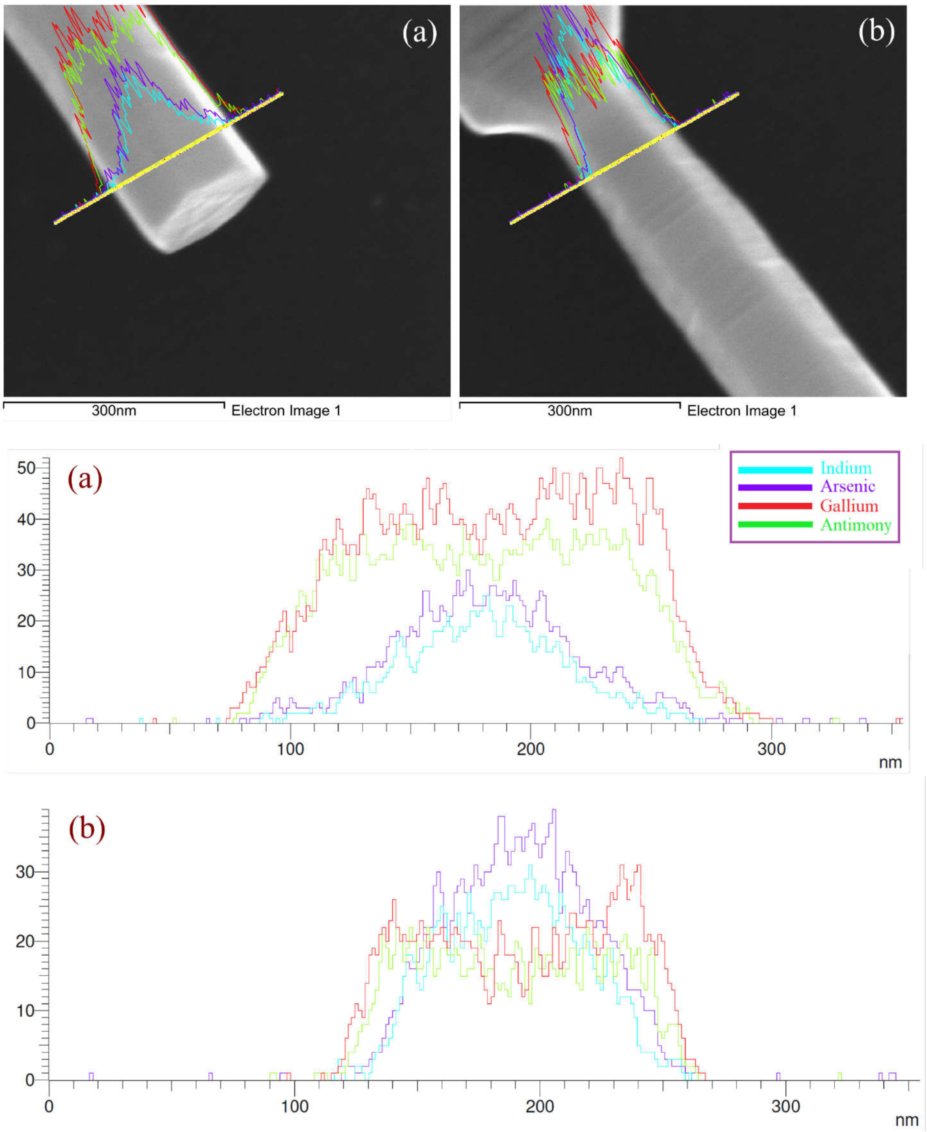


Figure 5.1: *EDX results for (a) top of the NW with a visibly thick GaSb shell and (b) the region of the NW with very thin diameter and thus possibly very little GaSb shell as seen in the corresponding scan.*

onto the inverse tapering and the formation of the pedestal like structure at the bottom, TEM could be conducted on different cross-sections of the NW to get a better estimate of the interface between the two materials and how it changes along the length of the NW.

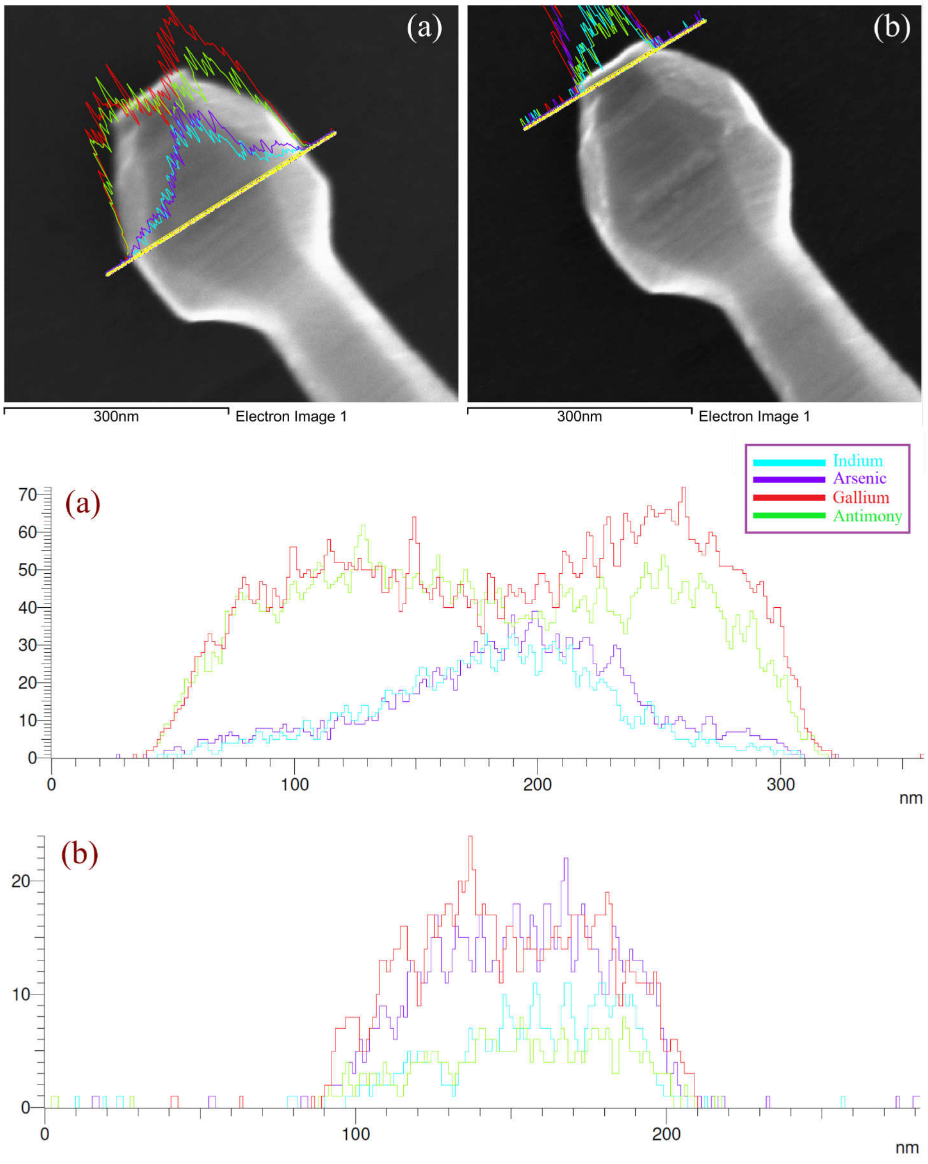


Figure 5.2: *EDX results for (a) the thick pedestal like structure at the bottom of the NW (b) the region of the NW with very thin diameter which was possibly inside the hole an thus unexposed to the impinging shell adatoms. The bottom display the corresponding scans showing the corresponding material composition*

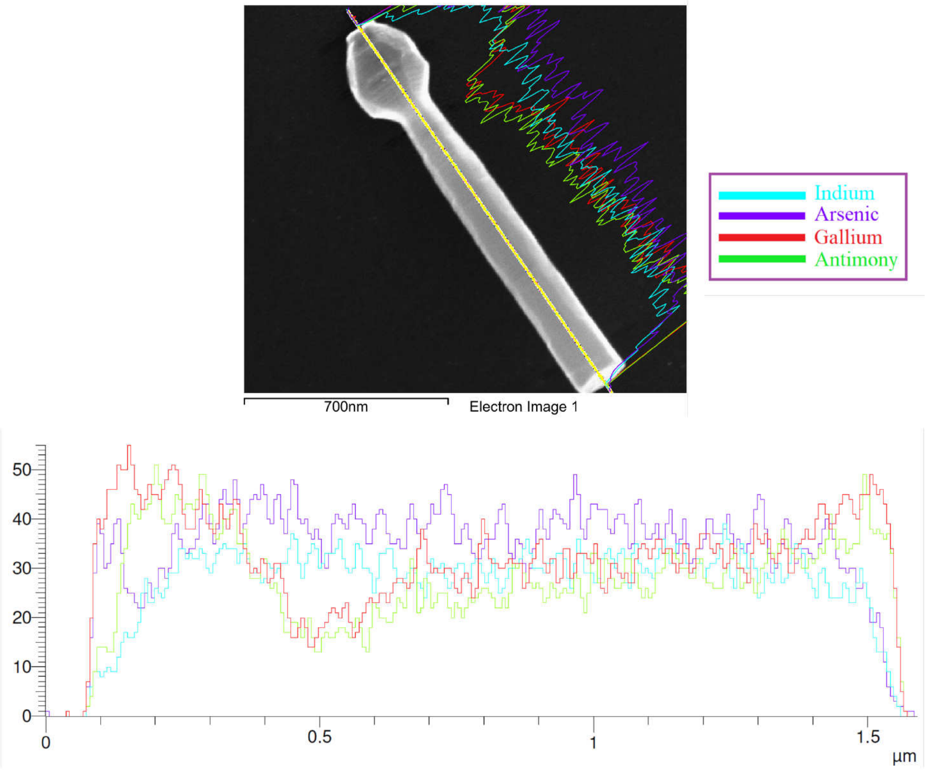


Figure 5.3: *EDX results along the length of the NW showing a sharp decline of the GaSb shell near the bottom of the NW just above the region of a very thick pedestal like formation comprising of Ga and Sb as can bee seen in the corresponding scan.*

Device Fabrication

There are things known and there are things unknown, and in between are the doors of perception.

- Aldus Huxley

6 Introduction

For the proper electrical characterization of the InAs/GaSb core-shell NWs, as well as the fabrication a lateral NW TFET, the device processing is crucial. This chapter describes all the steps involved in the successful device processing for measurements. Various tests were conducted to establish an optimized and reproducible process. All steps of the fabrication, just as for the substrate preparation for selective area growth of the NWs, were performed in the cleanroom (Helmholtz Nanoelectronic Facility, HNF) at the Forschungszentrum Jülich.

7 T-Gate 12 substrate

After growth, the NWs are mechanically transferred onto the substrate for device processing and measurements, a so-called T-Gate 12 sample. Details of the underlying computer-aided design (AutoCAD) layout are shown in Fig. 7.1. It is a 12 mm×12 mm (see Fig. 7.1 (a)) pre-patterned n-doped Si(100)substrate covered with 150 nm of SiO_2, which later served as the dielectric for back-gate dependent measurements. The fabrication of the T-Gate 12 sample is an already established process and is in use for most of the NW characterization in the institute. New T-Gate 12 wafers were processed during this work with the help of Patrick Liebisch and the corresponding process parameters can be found in his master thesis[35].

Each T-Gate sample consists of 24 fields fenced by Ti/Au bond pads (see Fig. 7.1 (b) and (c)) and hosts a Ti/Au marker 'graveyard' pattern in the center (see Fig. 7.1 (e) and (f)). This is to enable locating transferred NWs as well as for establishing contacts between the NWs and the bond pads during metallization in one of the following process steps. At the corner of every field there are six alignment markers as shown in Fig. 7.1 (d). Using these, multiple EBL steps can be aligned to each other on one and the same sample. The top-left image in Fig. 7.1 (a) shows a 'pump-field' which is used for alignment purposes during EBL. The distance from the central marker on this field to the individual markers surrounding each of the 24 fields is pre-defined in the system to perform EBL with nanometers precision.

7.1 Transfer of the NWs onto the T-Gate substrate

NWs are transferred onto the T-Gate in the cleanroom with the help of a tissue. A small piece of the tissue is cut to have a sharp tip. It is first gently rubbed onto the sample from which the vertical NWs are to be transferred. The NWs stick to the tip of the tissue due to the van der Waals forces acting between a very small surface area of the tip and the NW itself. This tip is then gently rubbed onto the T-Gate sample (always in the middle of the fields since it is desired to have the NWs positioned within the 'graveyard' marker field). The sample is then checked under the optical microscope to confirm if the NWs are deposited in the marker field. If too many NWs are transferred, it might not be possible to process individual NWs. In this case a clean tissue tip is rubbed over the 'graveyard' marker field in order to remove some of the NWs. The sample can be placed in acetone and ultrasonic sound can be applied to completely remove all NWs and start anew.

After the transfer of the NWs onto the T-Gate host substrate, high resolution SEM images of the graveyard field are taken to locate the transferred NWs. These images are used to align a further EBL process with the existing layout of the T-Gate for any kind of EBL processes on the NWs. In the following sections these are processes such as defining windows

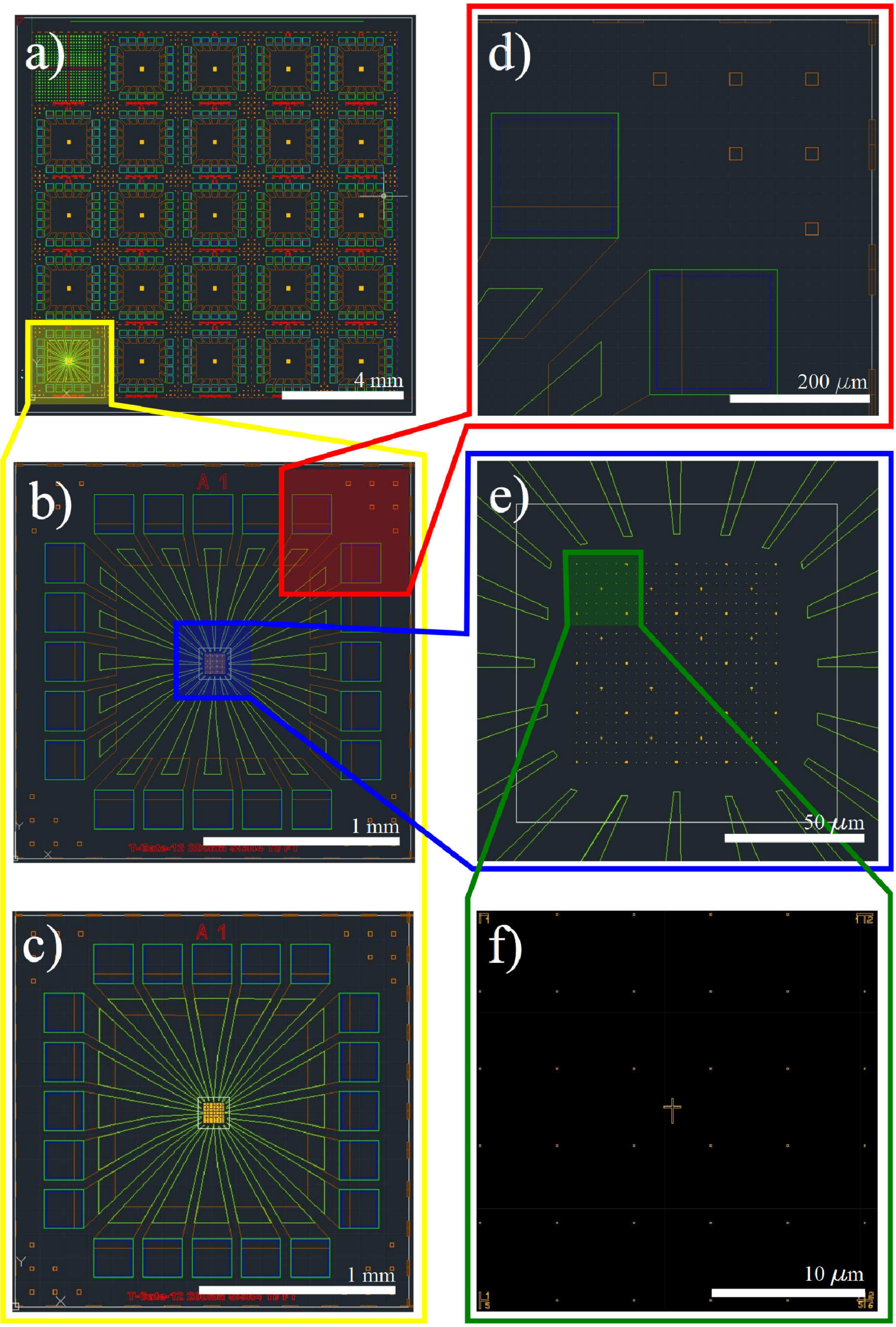


Figure 7.1: *Overview of the T-Gate substrate as defined in AutoCAD. (a) T-Gate substrate with 24 individual fields and 1 pump field. (b) and (c)show a single cell with different designs for the interconnects between the device contacts and bond pads, which have been modified to improve lift-off results. (d) Close up of the EBL markers, which are used for alignment of individual layers. (e) shows a close up of the center of the cell, where the 'graveyard' markers are defined. (f) Close up of one of the 'graveyard' marker fields.*

for selective etching, designing contacts, etc are described. Due to the ease of finding each NW that is wished to be processed upon with the markers on this substrate, all further tests for device substrate preparation were conducted on such T-Gate samples.

8 Selective etching of the GaSb shell

To have access to the InAs core of the NW, it is necessary to selectively etch the GaSb shell. In order to selectively etch the GaSb shell from parts of the NWs, the following approach is carried out. The NWs are transferred onto a T-Gate host substrate as explained in the previous section. After high resolution SEM images have been taken, an EBL design was created using the AutoCAD program. The NW SEM images thereby were overlaid and aligned with respect to the layout of the markers (see Fig. 8.1 (b) and (d)). Small windows on parts of the NWs have been defined as shown in Fig. 8.1 (b) and (c), in which the NW shell is to be etched selectively. After definition of the EBL layout the sample is then covered with resist to prepare for EBL. For EBL processing of the etching windows an AR-P 679.04 (950K PMMA) resist has been chosen. To ensure a better sticking of the resist onto the substrate and the NWs, HMDS (hexamethyldisilazane), which is a known primer for PMMA, is used. The detailed fabrication parameters involved in this process are displayed in table 10.1.

After development, the areas in the resist previously defined are now exposed and the sample is ready for etching. Fig. 8.2 shows SEM images of individual NWs after development with the defined windows in the PMMA resist. Three methods were tested to selectively etch the GaSb shell from parts of the NWs. An example of an etched NW is shown in Fig. 8.1 (e). The following section describes the three etching methods mentioned, two of them are wet etching techniques and the third one is a dry etching process.

A detailed study of the type of etchants that can be used for wet chemical etching was performed in[36]. Three etchants, namely, HF:H_2O_2 (in various dilution concentrations), a photo-resist, alkaline-based (TMAH - tetramethylammoniumhydroxid) developer called AZ 326 MIF, and NH_4OH were tested for their selectivity and effectiveness. It was concluded that the developer, with its 2,38% TMAH base worked best. Thus, this was tested again with respect to obtaining the etch rate and quality of etching.

8.1 Wet chemical etching with AZ 326 MIF developer

The etching of the GaSb shell in the AZ 326 MIF developer is isotropic. Fig. 8.3 shows the NWs on the host substrate after being dipped in the developer for 5, 10, 15 and 20 min (Fig. 8.3 (a), (b), (c) and (d) respectively). The sample is constantly stirred and then dipped in a DI water bath for 5 min to stop the etching process. As can be deduced from the shown images, the quality of etching is quite poor and the etch rate cannot be accurately

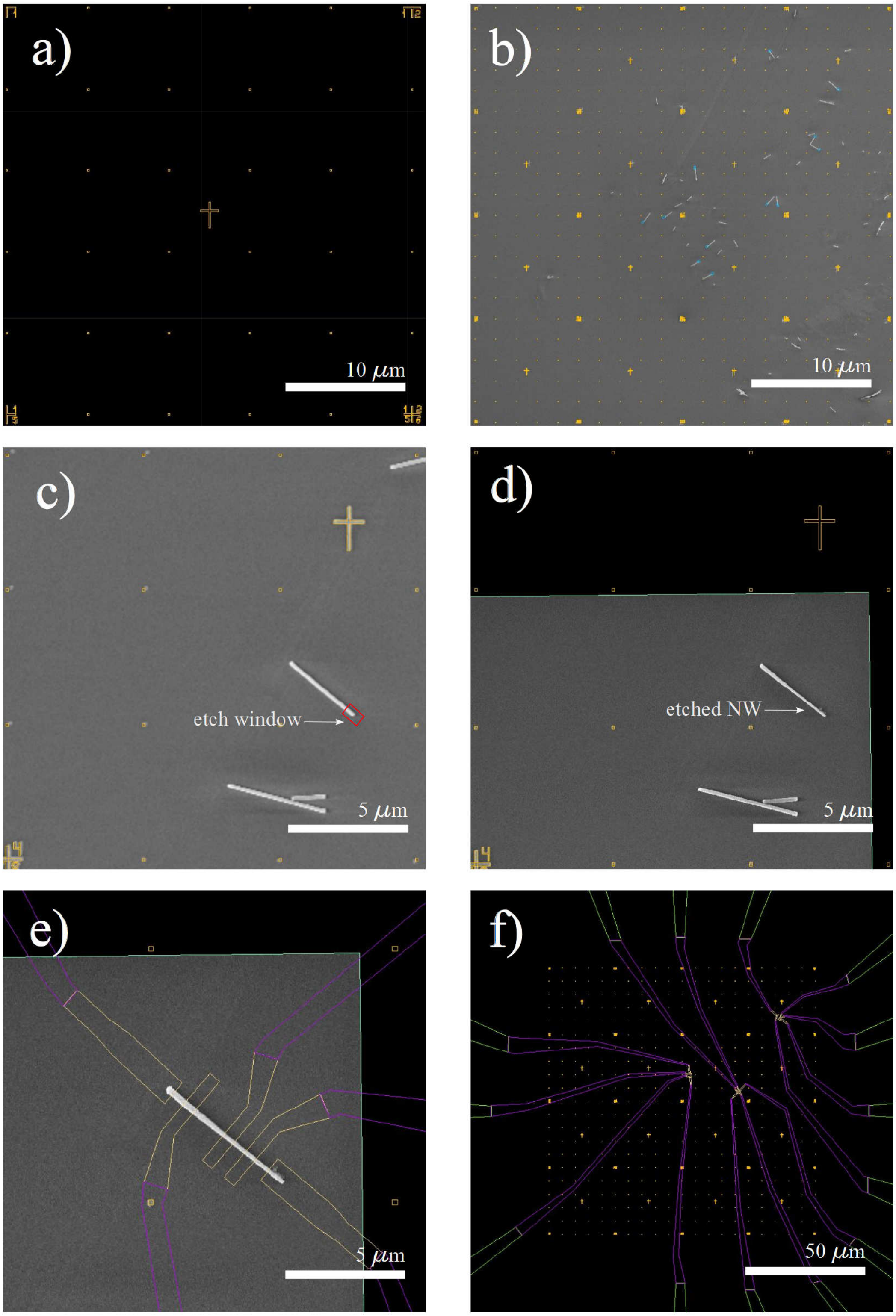


Figure 8.1: *Overview of the steps involved in designing windows for etching and contacts on NWs on a T-Gate. (a) The graveyard field in an AutoCAD design. (b) An SEM image of a sample with NWs aligned with the design, etch windows are then defined on chosen NWs. (c) close-up of one such etch window (d) SEM image of the same NW after etching aligned withe the design. (e) close-up of the contacts designed on the said NW. (f) An AutoCAD layout displaying one field with three NW contact designs*

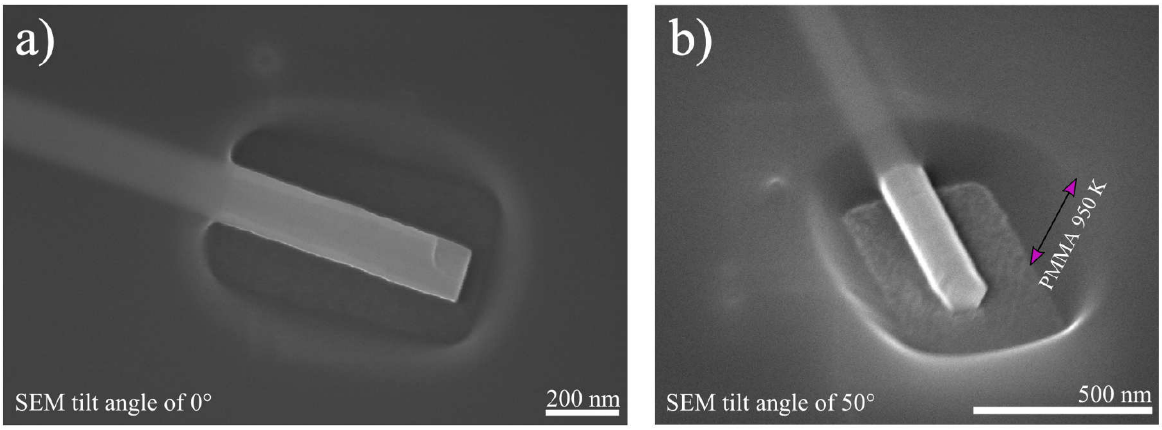


Figure 8.2: *(a) Top view SEM image after development showing the exposed part of the NW. (b) A tilted view displaying uniform coverage of the NW in the resist.*

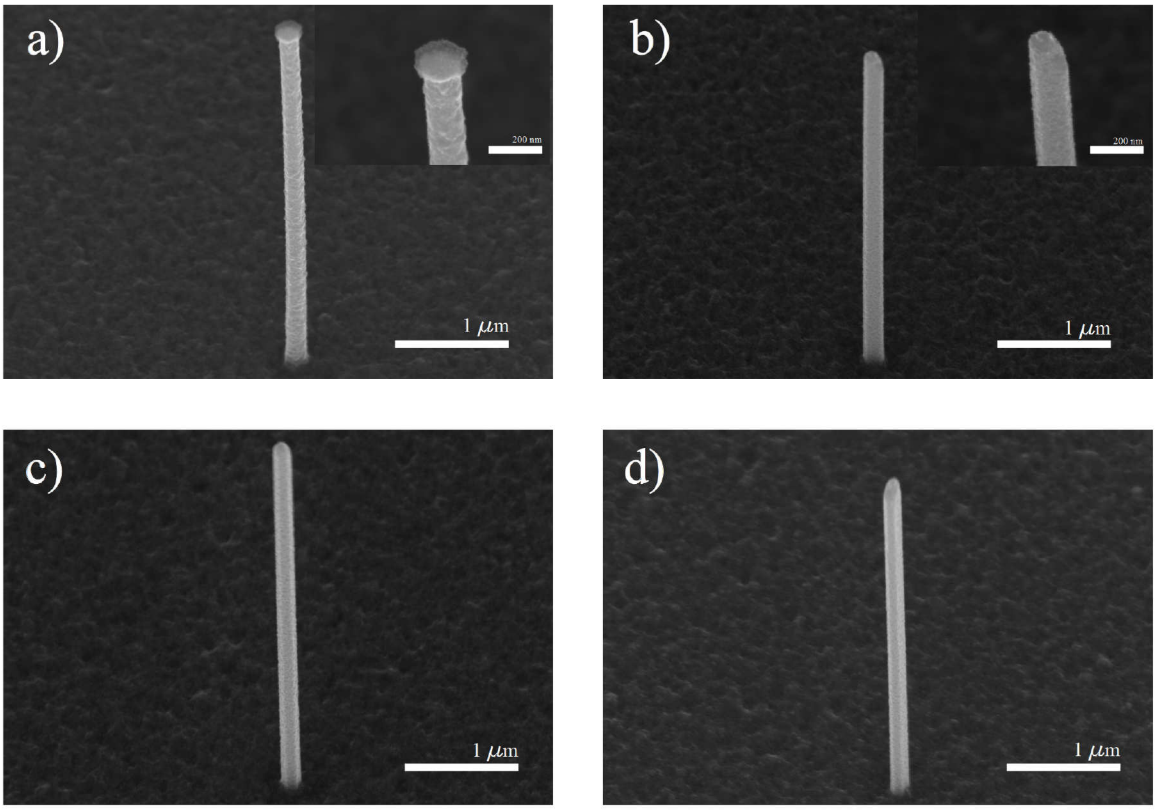


Figure 8.3: *GaSb shell etch results for (a) 5 min, (b) 10 min, (c) 15 min and (d) 20 min in the alkaline based AZ 326 MIF developer. The images have been taken at a tilt angle of 30°. In the inset of (a) and (b) close ups of the NW top. While after 5 min the GaSb hat is still visible it is not anymore after 10, 15 and 20 min.*

determined, since not much difference is observed in the morphology of these samples. The surface of the NW looks really rough, which might lead to poor quality of electrical contacts later. This etchant was eliminated from the possible etchants due to the quality of etching.

8.2 Wet chemical etching with NaOH

For this test, samples with pre-defined windows were used. Following the etching process from[13], NaOH was tested out as the next etchant. In this reference article, a really good selectivity of the GaSb shell was observed for similar NW dimensions. NaOH solutions have been prepared using Na-pellets dissolved in de-ionized water. Preliminary tests starting with 1.0 M NaOH showed the etch rate to be quite high and therefore subsequent etching tests were conducted using more diluted solutions. The main reason therefore is that an etch time of less than 15 s is prone to errors and cannot be reliably reproduced. Ellipsometry measurements were conducted on some of the test samples to check the effect of the etchant on the PMMA resist used. It was confirmed that exposure of the resist to the etchant for a few minutes does not change the resist thickness more than 5 to 10 nm. SEM images shown in Fig. 8.4 display the NWs etched in a 0.5 M NaOH solution for 15, 30, 45 and 60 s, respectively. As before, the etching is stopped by transferring the sample into a DI water bath for 10 min. As can be observed, 45 s (see Fig. 8.4 (c)) was optimal to remove the shell from the NW without leaving any visible remnants. The comparison of the diameter of the NW before and after etching confirms that the shell is completely removed for the desired part of the NW. While for etching times below 45 s the GaSb shell is not yet completely etched (see Fig. 8.4 (a) and (b)), for etching times exceeding 45 s the GaSb shell is completely removed on the whole NW (see Fig. 8.4 (d)). It was later observed that most of the NWs showed a slight gradient in the diameter which confirms that the etchant does seep through under the resist and continues to etch the shell a little longer. However, since the NWs are at least 4 μm long, the under-etching of a few nanometers did not affect the process.

The first attempt at removing the resist with regular solvents such as acetone surprisingly failed, especially with resist being observed to stay near the NWs. This was attributed to the fact that while taking SEM images of the sample after development, the constant exposure of the PMMA to an incoming beam of electrons changed its chemical structure with respect to polymer bond lengths and hardens it. This fact later makes it difficult to remove the hardened PMMA resist. Only a 200 sccm O_2 plasma etch with a power of 200 W for 2 min was successful in removing the resist. Thus, for all the samples after the first attempt, SEM analysis was deliberately avoided to later not have problems with the resist removal.

Furthermore, an energy dispersive X-ray (EDX) analysis was carried out to investigate the composition of the etched NWs. The EDX results are displayed in Fig. 8.5.

A comparison of the relative concentrations of In, As, Ga and Sb over the non-etched

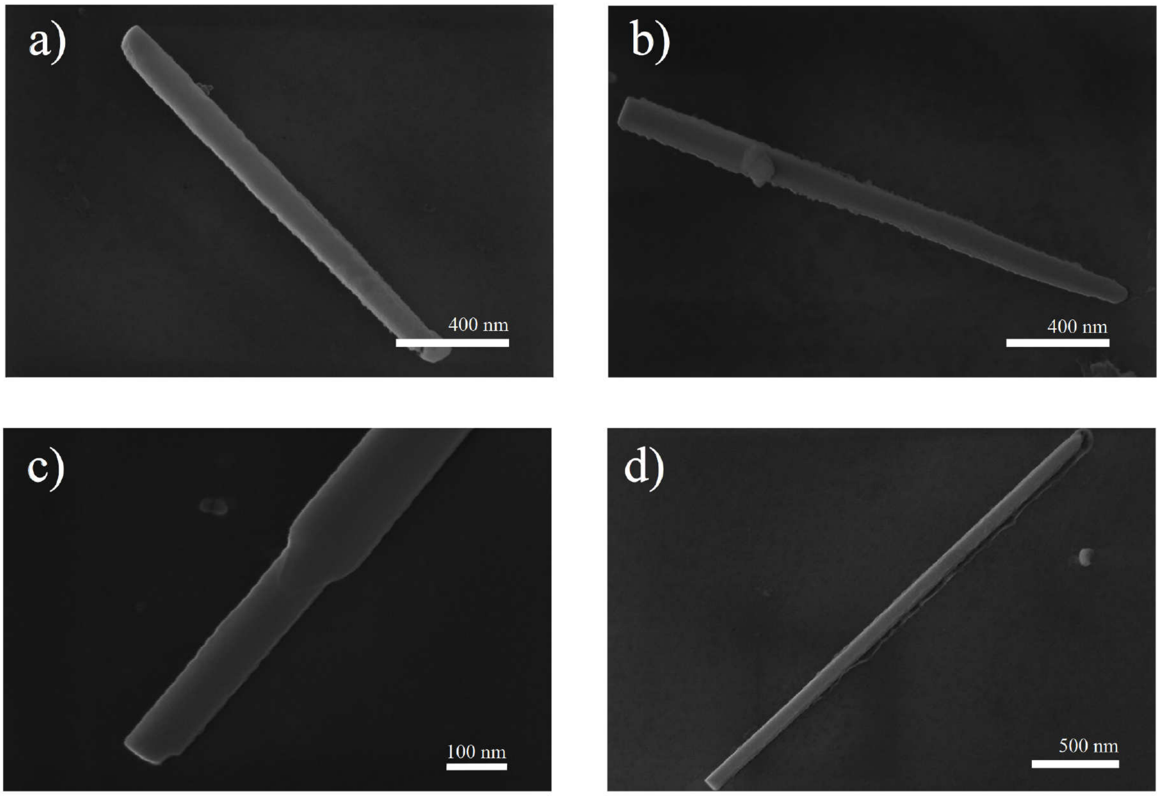


Figure 8.4: *GaSb shell etch results using NaOH for (a) 15 s where no change in the diameter indicates the shell is mostly unetched, (b) 30 s where a slight gradient in the diameter indicates the start of etching of the NW, (c) 45 s where a distinct change in diameter is observed for the part that has been etched and (d) 60 s where a completely etched NW is seen.*

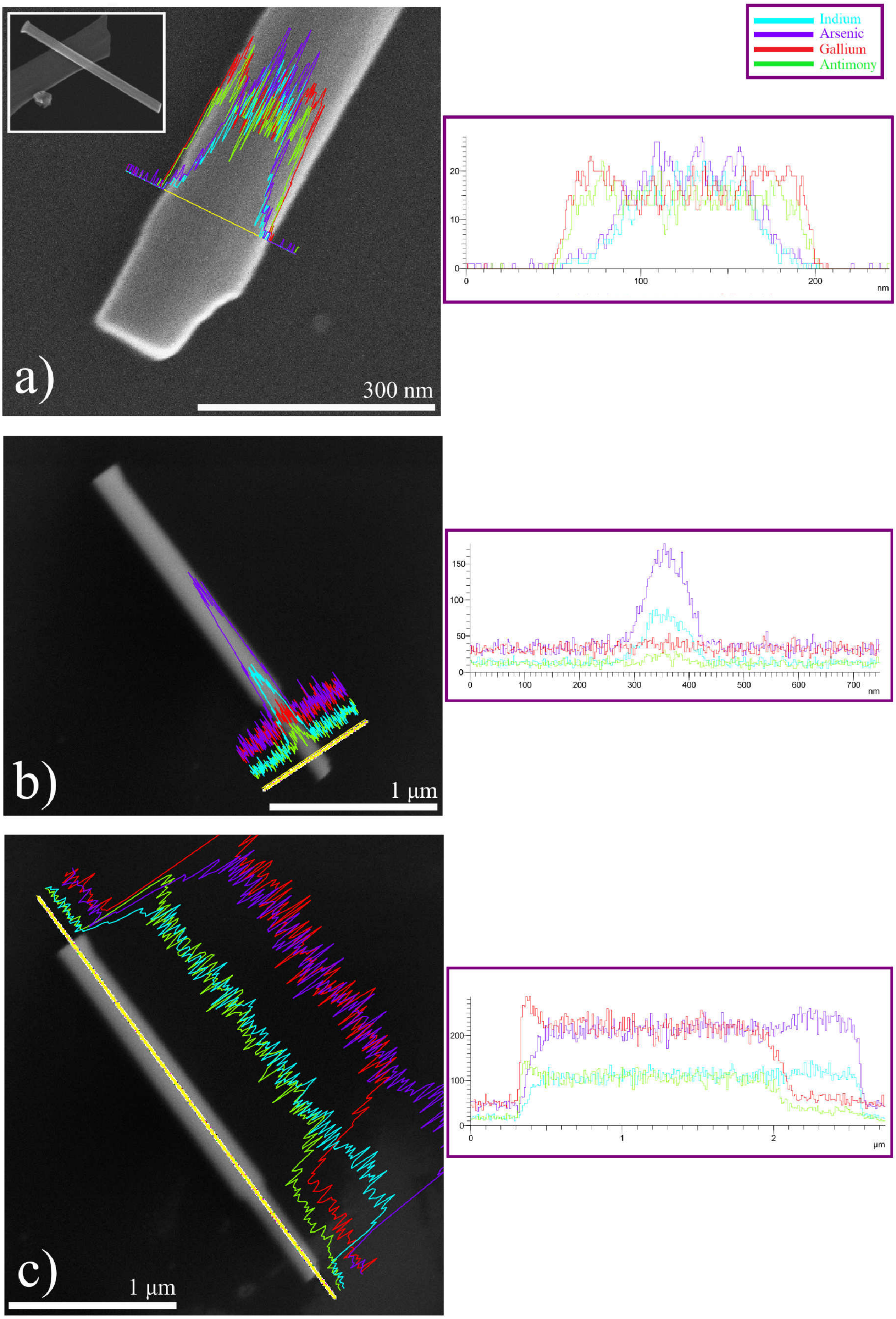


Figure 8.5: *EDX results of InAs/GaSb core/shell NWs. (a) A non-etched NWs showing a shell thickness of approximately 30 nm. (b) EDX scan over etched part of the NW showing very low Ga and Sb and high In and As content. (c) EDX scan over the whole length i.e., etched and un-etched parts of the NW*

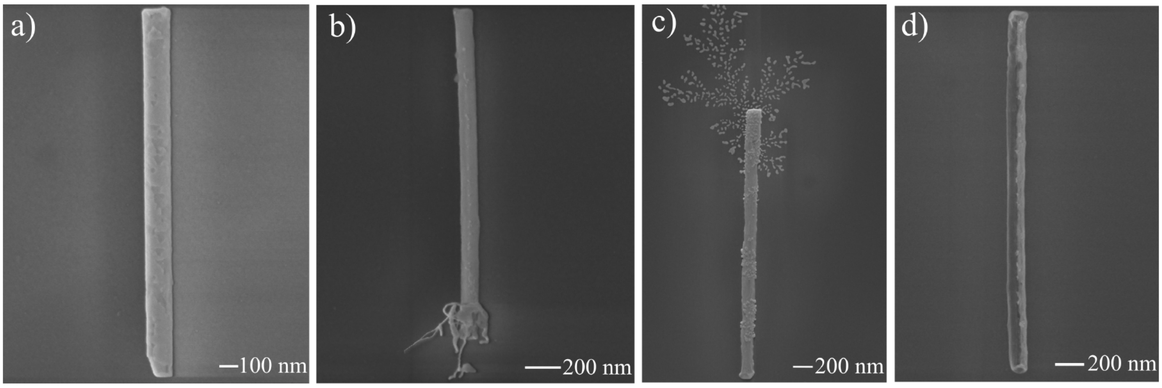


Figure 8.6: *GaSb shell etch results for (a) 30 s, (b) 60 s, (c) 70 s and (d) 80 s with the RIE. (a) shows very little material is etched, (b) and (c) better etching with possible residual GaSb deposited back onto the substrate and (d) shows a slight over-etch of the shell*

and etched part of the NW clearly shows a sharp decline in the Ga and Sb concentrations for the latter. Both scans, along the length of the NW (see Fig. 8.5 (c)) and transversal on the non-etched and etched part of the NW (see Fig. 8.5 (a) and (b)) show that 0.5 M NaOH indeed is a selective etchant that can etch the GaSb in an isotropic manner. The parameters for etching were checked for reproducibility and thus this method was used for the NW device fabrication.

8.3 Dry etching with RIE

Although, a wet etching technique to selectively etch the GaSb shell was established, anisotropic dry etching was tested out simultaneously to investigate qualitative differences. After following up on suggestions from the Oxford Instruments team, a dry etching was attempted using Cl_2 gas.

The inductively coupled plasma (ICP) system was used in the RIE mode with parameters: 30 sccm of pure Cl_2, 50 W forward power and 30 mTorr chamber pressure. As expected, due to the unidirectional nature of this etching process, only part of the shell exposed on top was etched and the part of the NW in contact with the substrate remained un-etched. The etch rate of PMMA in this process was checked with ellipsometry to be 10 nm/min. Fig. 8.6 shows SEM images displaying the etching results for a variation in etch time 30 (Fig. 8.6 (a)), 60 (Fig. 8.6 (b)), 70 (Fig. 8.6 (c)) and 80 s (Fig. 8.6 (d)). Certain advantages of the established dry etching over the wet etching process are that the former is more controlled and reproducible. However, due to the anisotropy of the process, leaving half of the shell intact, this method was not investigated any further. Possible ways to implement this process further would be to additionally use a wet etchant e.g., NaOH for a very few seconds after RIE etching and compare the results with the regular wet etching process described.

EDX analysis conducted on dry etched samples is displayed in Fig. 8.7 along, as well as perpendicular to the NW.

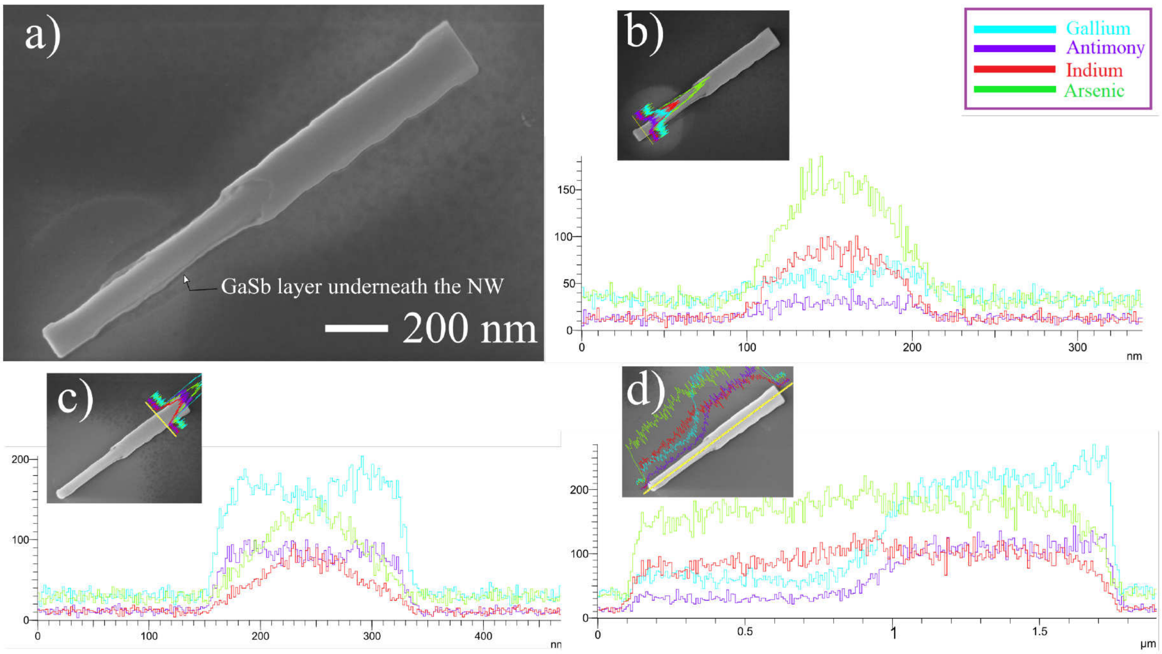


Figure 8.7: *EDX results from selective etching of GaSb shell using RIE. (a) An SEM image showing the isotropy of the RIE etching due to the left-over shell underneath the NW. (b) EDX scan over etched part of the NW showing only a slightly lower Ga and Sb content compared to the In and As content. (c) and (d) show scans over other parts of the NW*

9 Removal of native oxide

In order to achieve low resistance ohmic contacts on the NWs, it is essential to remove the native oxide from the surface of the NWs prior to metal deposition. It is known that GaSb is highly reactive and thus prone to oxidation[37]. For films, upon exposure to air, the surface forms a Ga-oxide (Ga_2O_3) and an Sb-oxide (Sb_2O_3) according to the reaction scheme in[37]:

$$\begin{aligned} 2\,\mathrm{GaSb} + 3\,\mathrm{O_2} &\longrightarrow \mathrm{Ga_2O_3} + \mathrm{Sb_2O_3} \\ 2\,\mathrm{GaSb} + \mathrm{Sb_2O_3} &\longrightarrow \mathrm{Ga_2O_3} + 4\,\mathrm{Sb} \end{aligned}$$

InAs/GaSb core shell NWs are expected to have a native oxide layer not more than 2 nm[34]. Pre-established methods[38] for removal of native oxide were tested out to check their effect on the NW morphology because this could, in effect, change the surface states and thus the electrical characteristics of the NW. In this section the effect of HCl with differing concentrations for and Ar-sputtering as direct removal of the native oxides are discussed.

9.1 With HCl

From[39], the first attempt to remove the native oxides was carried out with HCl:H_2O 1:3 for 30 s. First the sample is cleaned with acetone and IPA to remove contaminants gathered during other steps of the process. Afterward the sample is dipped in the HCl solution for 30 s and then rinsed with IPA and finally blown dry with nitrogen. However, on comparing the diameter of the NW before and after dipping in the solution, using SEM, it was observed that there was a significant decrease in the diameter of the NW implying that the shell was almost or in some cases even completely etched. Subsequently, further attempts were made with more diluted solutions starting with HCl:H_2O 1:5 until 1:30 but even the most diluted solution etched the shell completely and thus was deemed unusable. These results are displayed in Fig. 9.1. Thus, due to the highly reacting nature of GaSb, this option was eliminated.

9.2 With in-situ Ar sputtering

Since the NW surface is prone to re-oxidation from air, in-situ cleaning processes such as Ar-sputtering, just before metal deposition, are considered[38]. In[40], different plasma-assisted techniques prior to metallization, to remove the native oxide from epitaxially grown p-GaSb, have been reported. A comparison is even made with conventional chemical methods by

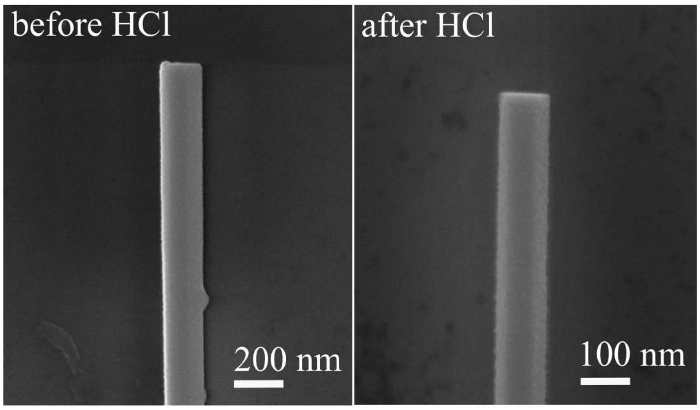


Figure 9.1: *The same NW before and after the HCl:H_2O 1:30 treatment for 30 s. The comparison of the diameter implies that the GaSb shell is completely removed even with the most diluted solution.*

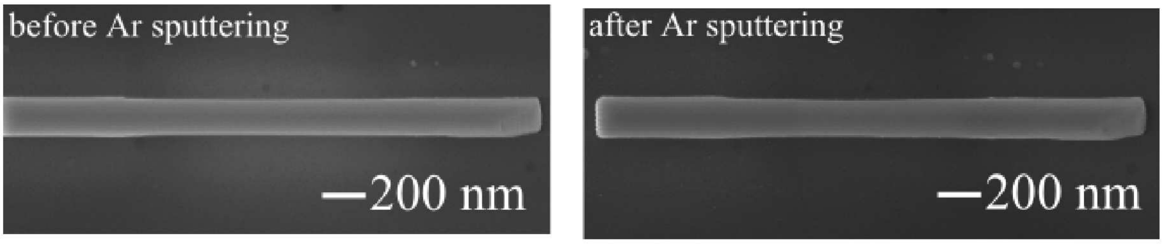


Figure 9.2: *The same NW before and after argon-sputtering for 30 s. No change in diameter has been observed and hence it has been concluded, that the GaSb shell is not effected during this treatment.*

evaluating specific contact resistances at the metal semiconductor interface. It is concluded that Ar^+ irradiation lead to extremely low contact resistances. The standard parameters of 80 V acceleration voltage, 2 A DC current and an Ar gas flow of 12 sccm are used for the tests conducted in this work. The effect after 10, 20 and 30 s of Ar-sputtering was tested. Fig. 9.2 shows SEM images of NWs before and after 30 s of Ar-sputtering prior to metallization. As seen from the SEM images, even 30 s do not seem to change the NW morphology with respect to its diameter or surface roughness. A sputter time higher than 30 s could not be tested since that might lead to etching of the GaSb after oxide removal and thus contaminate the metallization chamber dedicated to III-V materials.

10 Fabrication of metallic contacts on the NWs

After selective etching of the NWs, the best etched NWs are selected for the next step, i.e., deposition of metallic contacts. The AutoCAD design is now modified to make contacts from the bond pads of the T-Gate to the NWs for each of the 24 fields. The number of total contacts per field is limited to 20 because of the design of the sample, which on an average allows 4-5 NWs to be contacted per field. There are 20 contact pads in the T-Gate design, since the chip-carrier used for low-temperature measurements has a total of 20 DC connections.

The processing of normal metal electrodes on the InAs/GaSb core-shell NWs consists of several steps, schematically shown in Fig. 8.1 (e) and (f). First, the sample is spin coated with a three layer stack of PMMA. Then the sample is submitted for EB writing for defining the contact design in the resist. The sample is then developed and metalized. After metallization, the excess metal is removed from the sample by removing the resist which 'lifts' the metal on top of it. This step is called lift-off. Fig. 10.1 shows a schematic describing these steps and shows an exaggerated version of what the sample is aimed to look like.

Parameters from the work of Patrick Liebisch[35] and Fabian Haas[41] were used as a starting point. However, it was found that these pre-existing optimized parameters could not be reproduced, due to the very different dimensions of the NWs and availability of different evaporators at the time of their work. Thus, the process was modified for the NWs used in this work with several tests conducted with respect to the resist stack, EBL doses, thickness of the metal layers. Finally, a comparison in the quality of lift-off with two different evaporators to deposit these metals was done. Investigations and results are discussed in the following sections. The optimized process parameters can be found in table 10.1.

10.1 Resist stack

Th parameters from the work in[35] did not produce good metal contacts since his process was optimized for InAs NWs and the metal layers used were also different. The resist stack which finally produced good results was a modified version of the work in[41]. The first two of the three layer PMMA stack were AR-P 649.04 200K and the third layer was AR-P 679.04 950K. The first two layers were spin coated with a rotational speed of 4000 rpm, resulting in 120 nm resist thickness for each 200 K layer, and the third one at 6000 rpm, resulting in a

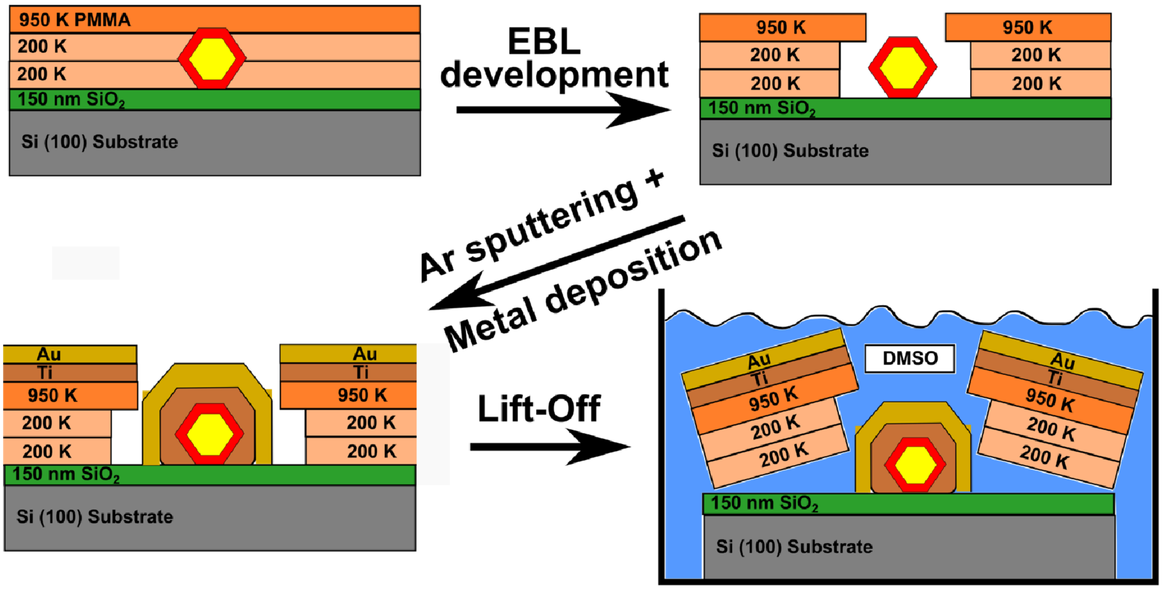


Figure 10.1: *Schematic of the steps involved in the metal deposition process. The first picture shows the T-Gate sample with the NW covered with a three layered resist. After EB writing and development, a slight undercut in the resist stack is obtained due to the two types of resist. The sample is then submitted for evaporation of Ti and Au after it is first sputtered with Ar for 30 s to remove the native oxide. After metal deposition, the sample is put in an acetone (later DMSO, refer to section 10.5) bath overnight for lift-off.*

220 nm thick 950 K resist layer. Each layer was soft-baked at 90 °C for 60 s and hard-baked at 180 °C for 10 min. This post-bake process is performed in two steps to ensure that there is not a sudden increase in the temperature, which might lead to extra hardening of the PMMA, which could cause problems with lift-off later. It was ensured that the sample was allowed to reach room temperature in-between the application of each layer. The reason for using a multi-layer resist stack is to obtain an undercut in the first two layers of the stack. The two types of resist vary from each other with respect to the in the molecular length of the polymer it contains. Thus, the same exposure of electrons during EBL, changes this length differently for the two resists. In this case, the 200 K develops slightly more than the 950 K. This leads to the formation of the aforementioned undercut as shown in the schematic in Fig. 10.1. This later enhances the coverage of the metal around the NW and improves lift-off.

Since only the quality of lift-off was to be analyzed, these tests were conducted on bare Si(100) substrates with no NWs. All samples were deposited with a Ti/Au bilayer. Furthermore, the effect of 10, 20 and 30 s of Ar-sputtering was checked to see if it damaged the resist stack. It was found to have no impact on the quality of lift-off and thus all further samples were Ar-sputtered for 30 s.

Fig. 10.2 shows microscope images of these test samples after lift-off. The overall thickness of the resist stack for this system is 460 nm. This worked in favor of obtaining good contacts later on real samples with NWs since to obtain uniform coverage the thickness of the resist stack needed to be more than the diameter of the NW itself. Further tests with respect to EBL doses and Ti/Au bilayer thickness were conducted on this resist stack.

10.2 Tests with EB dose

Following the work of[35], the starting point for the EB dose was chosen as 2350 μC/cm^2. Higher doses were used compared to previous works so that the development could be conducted in one step[42]. For relatively lower doses, the development was optimized with the use of AR 600-55 for 70 s which is then stopped by immediately transferring the sample into an IPA bath and then blow-drying it. However, for relatively higher doses, the samples were developed in only IPA for 120 s and then blow-drying them.

For all the test samples (including the ones where the resist stack was being tested), a dose test was conducted above and below the value of 2350 μC/cm^2. This was with a starting value of 1962 μC/cm^2 in increasing steps of 3% for each of the 24 fields until 2826 μC/cm^2. A microscope image of one such sample with varying doses is shown in Fig. 10.3.

When the sample was checked under the optical microscope after development, different parts of the sample did not show a major difference, however, when the samples were checked it the SEM, the field with 2232 μC/cm^2 was found to be consistently the best. Thus, this was chosen to be the EB dose for the fine as well as coarse structures for samples with NWs.

10.3 Tests with metallization

A Ti/Au (CMOS) and Ni/Au (Esaki) bilayer system is known to integrate well with InAs/GaSb core-shell NWs. Since only Ti/Au was available in the deposition systems during this work, only this combination was used henceforth.

Ti is used to allow a good sticking of the Au on the substrate in general and the NW, as the Au does not form a closed layer on its own. Thus, for this to work a first test was conducted to check the minimum thickness of Ti required to cover the NW uniformly. Fig. 10.4 show top view and tilted images of the NWs covered solely with a 5 and 10 nm Ti layer. The thickness of the metal deposited always includes a slight error with each run, and the smaller the desired thickness the larger is the relative error. It was concluded that the samples with relatively thinner Ti layers, there were problems with Au not sticking to the NW and the metal being completely lifted; and with relatively thicker Ti layers, the metal was not lifted. Thus, 30 nm of Ti proved to be a reasonable value to try on the NW samples to ensure proper coverage of the NW for better sticking of Au and also not cause problems during lift-off. The Au layer was chosen to be 150 nm thick which makes the overall thickness of the metal contact 180 nm. It is essential that the metal bilayer thickness is more than the diameter of the NW which is in the range of 140 nm-150 nm.

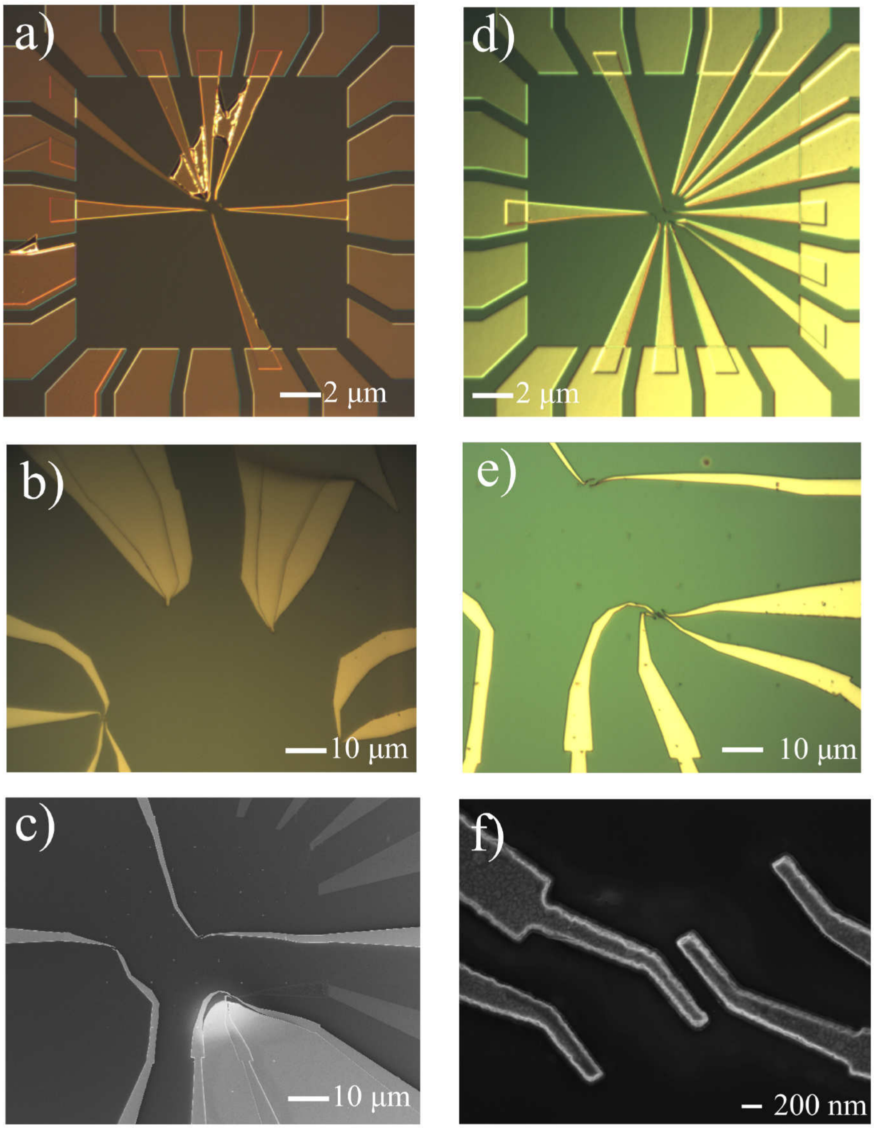


Figure 10.2: *A comparison between how the quality of lift-off looks before and after optimization. Figure (a) shows an optical microscope image of a field where metal in between the adjacent bindings did not lift completely, (b) is a zoomed in image of the same sample and (c) shows an SEM image of the same. Figures (d), (e) and (f) show in the same sequence a sample where the metal lifted properly. The difference in both samples is the resist stack that was used.*

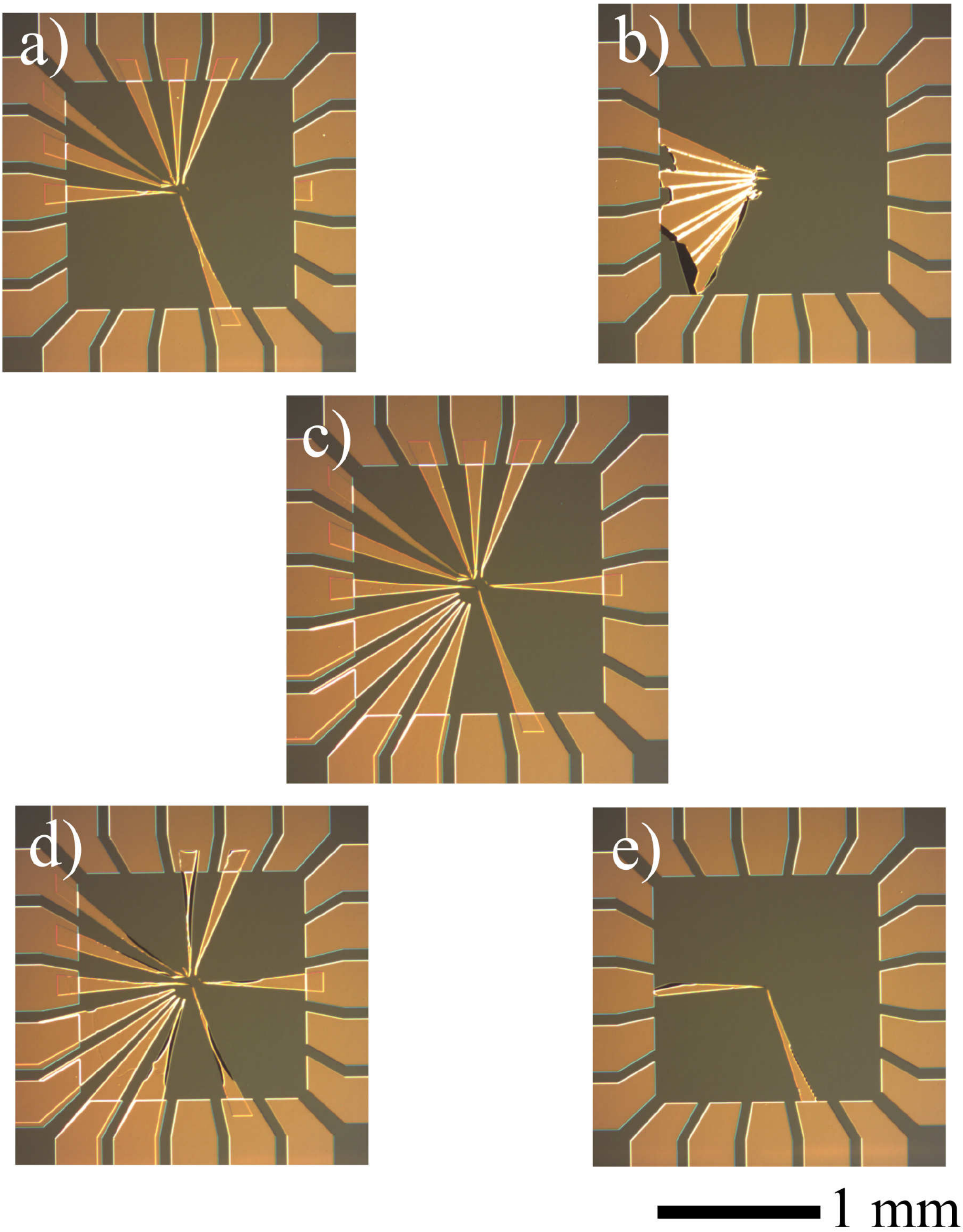


Figure 10.3: *Overview of the optical microscope images of the samples on which an EB dose test was conducted. The figures (a) and (b) are exposed to relatively lower doses which resulted in excess metal remaining on the sample, (c) shows a sample where the metal was lifted perfectly (this was the dose used later), and (d) and (e) are exposed to relatively higher doses which resulted in most of the metal being lifted off of the sample.*

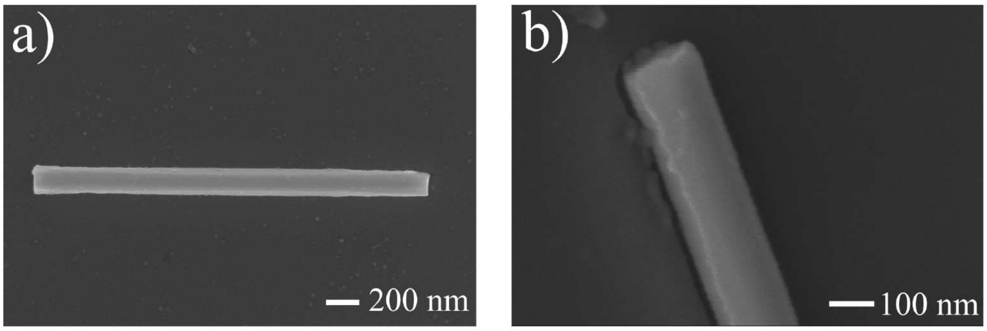


Figure 10.4: *(a) shows a top view SEM image of NW covered with 5 nm of Ti. As can be observed this thickness isn't enough for it to form a closed layer. (b) shows a 45 ° tilted SEM image of a NW covered with 10 nm of Ti. The increase in the thickness of Ti deposited forms a closed layer on the NW, however, the shadow in the deposition shows it is still not enough to form a closed layer all around it. Thus, a Ti layer of 30 nm was later used.*

10.4 Tests with evaporators

Due to some persisting problems with lift-off while multiple parameters for NW contacts were being tested out, it was essential to eliminate the metal deposition systems as the source of the problem. The two evaporators in the cleanroom that are dedicated to III-V materials have different geometries with respect to the relative position of the sample holder and the source material. Univex 400 is a system that allows deposition of the material from only one direction whereas PLS 500 allows for conformal deposition by rotating the sample during metal evaporation. Both systems at the time of this work were equipped with Ti and Au, however, only Univex 400 allowed for in-situ Ar sputtering before metallization. Thus, even though PLS 500 could eventually not be used for samples with NWs, to have a clear picture of the source of the problem it was necessary to compare samples processed with the same parameters in both systems.

This test was conducted simultaneously with the previous tests. Both samples were deposited with a 30 nm Ti and 150 nm Au bilayer. Fig. 10.5 shows that no difference could be observed in between these samples. Thus, the previous parameters were optimized instead.

10.5 Lift-off

Another parameter that was tested simultaneously along with the others was the solvent used for lift-off. After metallization, the sample was scratched with a tweezers around the edges to facilitate the start of the lift-off. The standard process included use of an acetone bath in which the sample was laid overnight to ensure a thorough dissolving of the resist to be able to lift the unwanted metal off of the sample. It was found that with the previously optimized process parameters, the lift-off quality was not always reproducible. As per the work of Jalil Abdul Rahman (unpublished), Dimethyl Sulfoxide (DMSO) was tested out

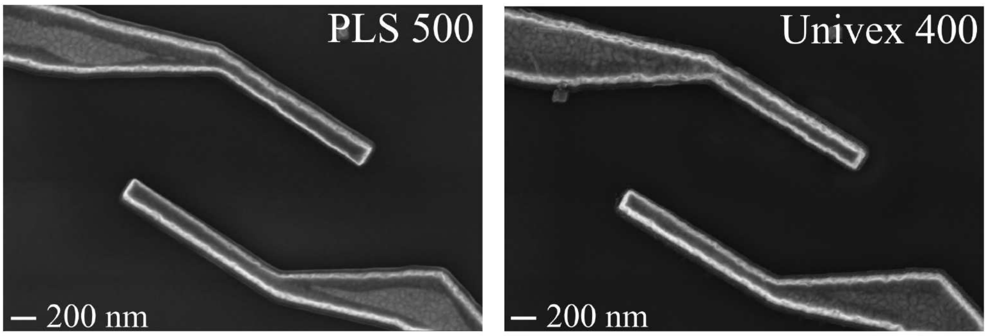


Figure 10.5: *SEM images showing two samples processed in different metal deposition systems for comparison. They show a single field with Ti/Au contacts with preAr-sputtering of 30 s. No difference was observed in the quality of the contacts as seen in this image.*

for lift-off on some test samples. After switching the solvent used from acetone to DMSO, the lift-off was 100% reproducible. A possible explanation is the DMSO is more viscous than acetone and dissolves the resist slower and less aggressively than acetone. The viscous nature would ensure that the resist expands slightly prior to dissolution and this in turn ensures that the metal above this resist is lifted properly. Together with the previously mentioned optimized parameters final samples with NWs have been prepared with metallic contacts for electrical characterization of the NWs.

10.6 Final parameters

Fig. 10.6 shows SEM images of test samples with no NWs with perfectly lifted contacts. Thus, it was concluded that parameters optimized in the previous sections indeed were reproducible and could be used for samples with NWs.

First, samples with un-etched NWs were contacted. This was done because in the work of[39], attempts to contact InAs/GaSb core-shell NWs with Ti/Au, Ni/Au and Pd/Au were deemed unsuccessful due to diffusion of the shell into the metal or an electrochemical reaction which lead to vanishing of the GaSb shell. However, no such effect was observed in this work and the previous unsuccessful attempt at contacting this kind of NWs was attributed to faulty fabrication.

Fig. 10.7 displays the SEM images from the first successful fabrication of NW contacts. The samples were later used for electrical measurements. After this, the same parameters were used to fabricate devices with etched NWs and contacts placed on both materials. Fig. 10.8 displays these various NWs that were also later used for electrical characterization. The choice to put several contacts on the NW was to facilitate several kinds of measurement. Multiple contacts on both InAs and GaSb are placed so that IV characteristics of different part of the NW can be investigated. This is one way to probe the hetero-interface between the two materials. Several samples with differently doped shells were fabricated to have the

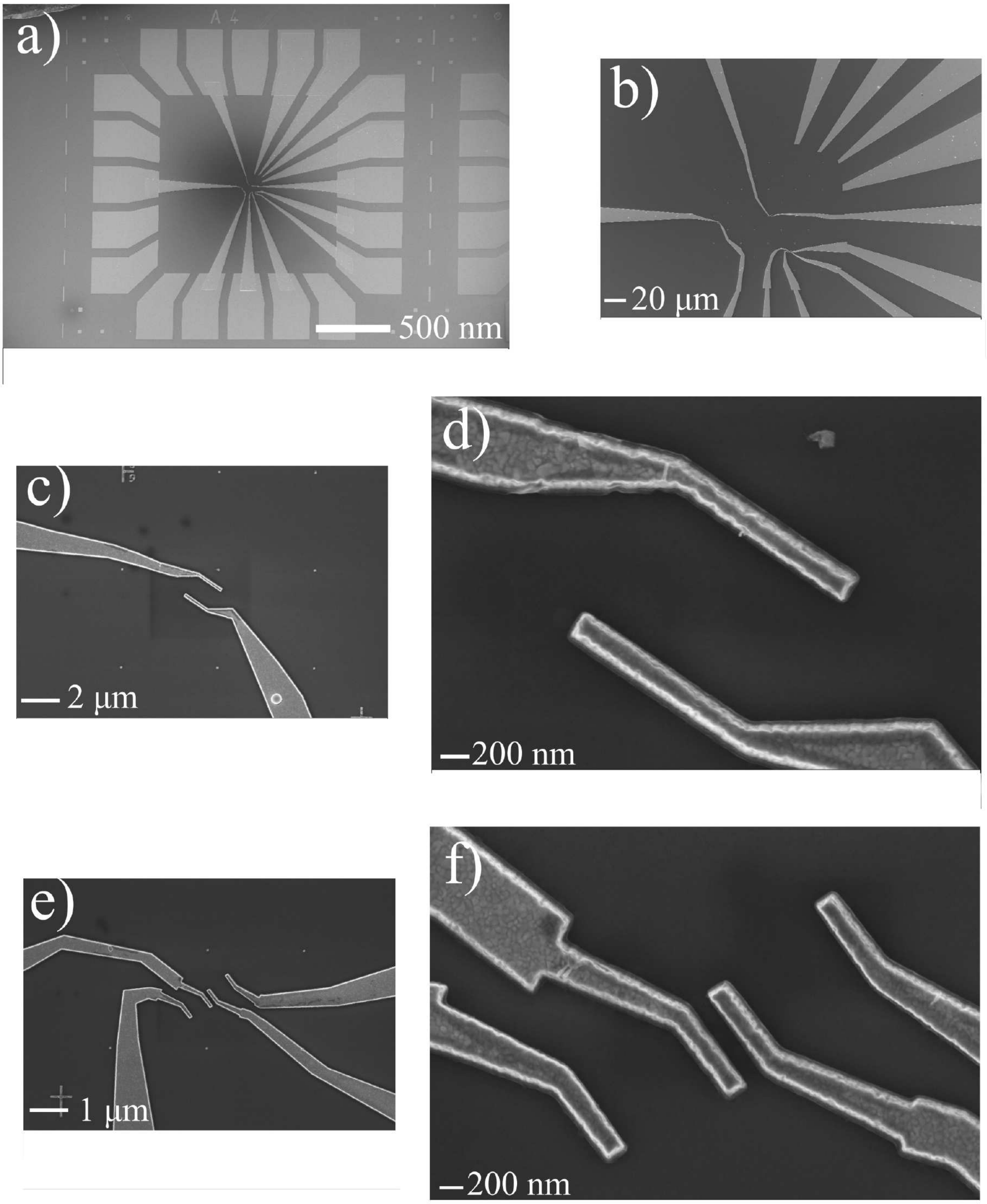
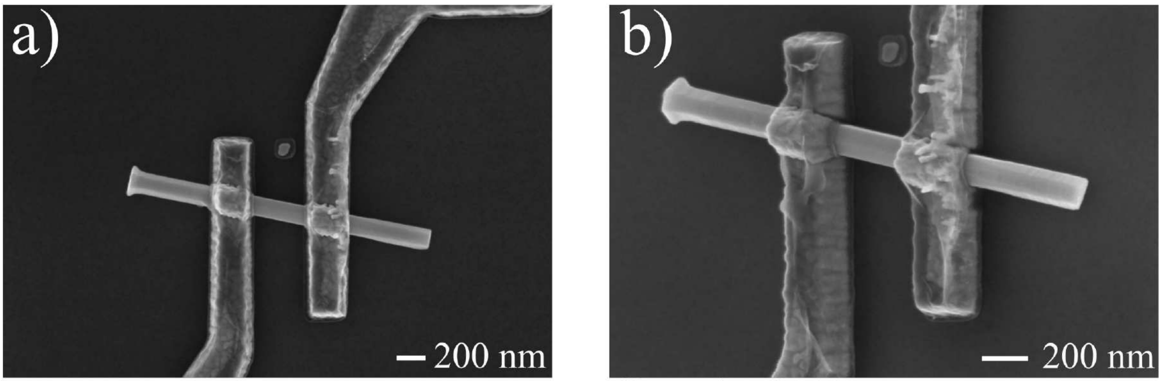
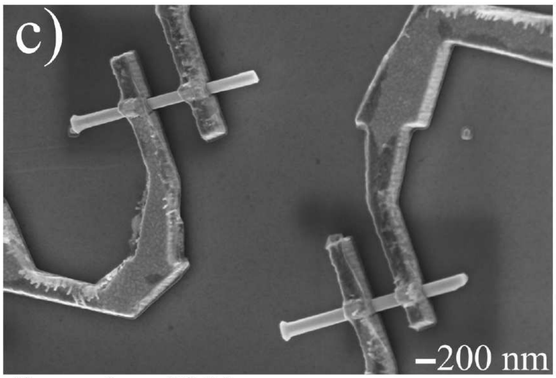


Figure 10.6: *Overview of SEM images of a sample processed with all the optimized parameters. (a) shows an overview of a single field and (b), (c), (d), (e), and (f) are zoomed in images showing different contacts on this field.*



top view

tilt angle of 30°



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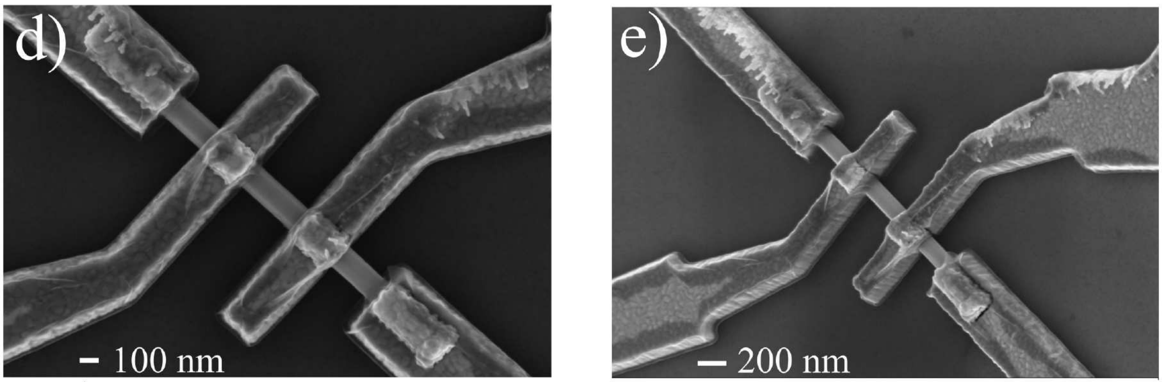

top view

tilt angle of 30°

Figure 10.7: *Overview of SEM images of successful deposition of metal contacts on InAs/GaSb cor-shell NWS. a) Top view of a two-point contacted NW, b) a tilted view showing uniform metal coverage around the edges, c) tilted view of two NWs on the same sample d) top view of a four-point contacted NW and e) a tilted view showing the same NW*

possibility to compare the effects of different doping concentrations.

A detailed analysis of all the parameters involved in selective etching of the NWs and processing metal contacts to them was presented. It was demonstrated that only a careful study of individual parameters can lead to a reproducible process and that these are also device dependent. Table 10.1 summarizes the final optimized parameters used for the device processing.

EBL step	selective area growth	windows for etching	NW contacts
pre-treatment	Ace/IPA clean 5 min, 110 °C	Ace/IPA clean 5 min, 110 °C	Ace/IPA clean 5 min, 110 °C
HMDS	-	130 °C	130 °C
resist used	AR-P 679.04	AR-P 679.04	AR-P 649.04 AR-P 649.04 AR-P 679.04
spin-speed (min^{-1})	6000 rpm (30 s)	4000 rpm (45 s)	4000 rpm (60 s) 4000 rpm (60 s) 6000 rpm (60 s)
softbake	10 min, 180 °C	10 min, 180 °C	1 min, 90 °C and 10 min, 180 °C
EBL dose	350 μC/cm^2	400 μC/cm^2	2232 μC/cm^2 (fine and coarse)
beam-current	1 nA	1 nA	1 nA (fine) 150 nA (coarse)
EBL step-size	2.5 nm	2.5 nm	2.5 nm (fine) 50 nm (coarse)
development time (s)	70 s	70 s	120 s
resist removal	Ace/IPA clean	Ace/IPA clean	DMSO/IPA

Table 10.1: *Fabrication parameters after optimization, for substrate preparation for selective area epitaxy of NWs and for fabrication of metallic contacts onto the NW*

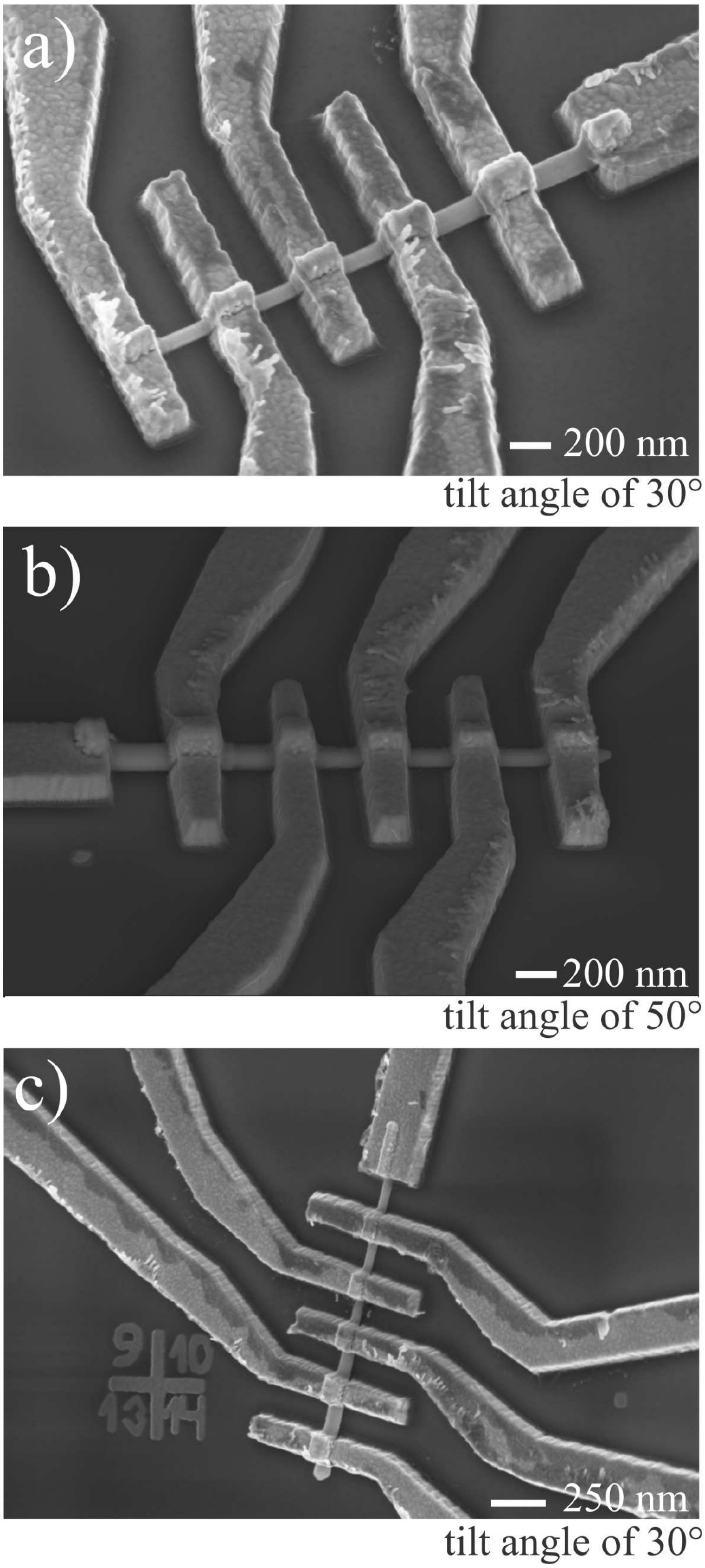

Figure 10.8: *Tilted SEM images of etched InAs/GaSb NWs with two contacts on GaSb shell, one contact on a slightly etched GaSb shell and two contacts on the InAs core. The GaSb shell is C-doped in (a) and (c) is with a doping concentration of* 1.25×10^{19} cm^{-2} *and b) is with a doping concentration of* 6.25×10^{18} cm^{-2} *corresponding to GaAs layers*

11 Dicing and bonding of the sample

Some preliminary measurements were carried out at the room temperature four probe setup at the PGI-9 IT. After these preliminary studies the measurements in this work were conducted in a cryogenic setup at Prof. Thomas Schäpers' laboratory (Magnet-lab). This setup did require for the sample to be cut and glued onto a chip carrier for measurements. The sample dimensions to be able to use this setup for any kind of measurements are restricted to the size of the sample holder. Thus, the sample needed to be diced into 2 mm×2 mm pieces. Prior to dicing, to protect the structures on the sample from external contaminants or scrap material from the dicing saw, the samples were spin coated with a thick layer of AZ 3214A resist and soft-baked at 100 °C for 5 min. After dicing, the cleaning of the cut pieces was done in a standard acetone and IPA solutions followed by blow drying them with a nitrogen gun. Then the individual cut pieces were glued with a conductive silver paste onto a ceramic chip carrier. These chip carriers provide 20 terminals, which can individually be contacted for measurements. While gluing the individual pieces, the piece was rotated in such a way that the NW could be aligned parallel to the known direction of the magnetic field inside the cryostat. After gluing the samples into the chip carrier, aluminum bond wires were used in order to ensure an electrical contact from each individual terminal of the chip carrier to the contact pads on the sample itself.

Measurements and Results

Many people find bald, unvarnished truths so disturbing, they prefer to ram their heads in the sand and start dreaming at the first sign of scientific reality.

- Charlie Brooker

12 Introduction

After the successful fabrication of the metal contacts on the NWs, several measurements were conducted on these samples. In this chapter, the electrical characterization of partially etched and non-etched InAs/GaSb NWs is discussed. DC characterization and magneto-transport measurements are useful in determining the transport mechanism of this complex material system. Measurements were conducted at room temperature and at low temperature using a cryogenic setup. The first part of this chapter describes the measurement setup, such as the cryostat working principle, the electrical setup and how the various types of measurements were conducted by use of this electrical setup. The next part of the chapter describes the various measurements performed and their analysis. In the last part of the chapter ideas are put forth for future measurements that could be conducted to obtain more information about these NWs and how these can be realized.

13 Measurement setup

13.1 Cryostat

Measurements at low temperatures were performed in an OXFORD variable temperature insert (VTI) fridge. This traditional wet system is schematically shown in the Fig 13.1. A detailed description of this setup can be found in Christian Weyrich's Ph.D. thesis[43]. In this section, only the most important aspects of operation will be discussed. The cryostat's sample chamber is positioned inside a dewar, which contains a superconducting coil for application of a magnetic field (B) and which is used to store liquid Helium (^{4}He). To reduce thermal exchange between the surroundings and the ^{4}He bath in the dewar, which contains up to 60 l of ^{4}He, an outer vacuum chamber (OVC) is used for isolation. Another, inner, vacuum chamber (IVC) is employed to isolate the sample chamber from the ^{4}He dewar. Due to the isolation of the sample chamber from the ^{4}He bath, temperatures below 4.2 K are also achievable. This is done by transfer of the ^{4}He from the bath to the sample chamber through a needle valve and constantly evacuating the He vapour out of the sample chamber. By controlling both the amount of ^{4}He being transferred inside the chamber and the rate at which the ^{4}He evaporates, it is possible to obtain temperatures down to 1.5 K. For temperature dependent measurements above 1.5 K and for temperatures lower than 50 K, a heater connected to the dipstick is used. Also by adjusting the needle valve during cooldown, temperature dependent measurements can be conducted above 50 K. Room temperature measurements can be performed by placing the dipstick inside a plastic tube setup next to the cryostat. As mentioned before, the ^{4}He dewar contains a superconducting solenoid which can produce magnetic fields up to 14 T. Since the geometry of the setup is such that the solenoid coil is wrapped around the sample chamber, the magnetic field produced is at the center of the sample chamber and along its axis. According to[43] its inductance of 100 H limits the ramp rate of the magnet to 0.5 T/min. An OXFORD IPS 120 A power supply is used to control the current applied to the magnet.

13.2 Dipstick and sample holder

For this work, a rotatable dipstick was used. It is equipped with a stepping motor, enabling rotation of the sample holder in an angular range of -10° to 100°. This permits with respect to the magnetic field axis, an in-plane magnetic field at 0° and a perpendicular out of plane magnetic field at 90° and additional 10° freedom of rotation in both directions. The dipstick is also equipped with a temperature sensor that is read-out by a temperature controller which controls the heater. To connect the temperature sensors as well as the 20 DC connections on the sample holder to the head of the dipstick, a 12-pair Constantan Loom cable is used.

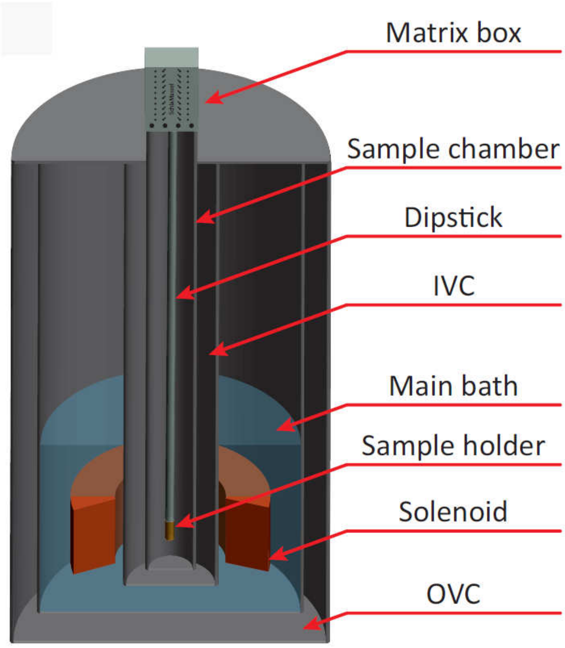

Figure 13.1: *Schematic cross-section of the cryostat from[43]*

For noise reduction, RC filters shortly before the sample holder are facilitated. These RC filter elements are based on surface mounted device (SMD) capacitors and resistors. The resistors are designed for ultra-low temperatures using a passivated nichrome layer, which has a temperature coefficient of resistance (TCR) of just 5 ppm/°C. The capacitors are also chosen regarding their low change capacitance over temperature value of just 30 ppm/°C. More details about the individual components of the VTI cryostat and how the setup was designed to obtain optimum readout values can be found in[43].

13.3 Electrical setup

For all measurements, the following describes a list of devices that were used for electrical characterization: Keysights 3440 A Multimeters, Stanford Research SRS830 Lock-in Amplifier, HP 3245 A Universal Source, Keithley 2400 Source Meter Unit (SMU), and devices built in-house namely, a PGI-box, a MATRIX box and a STAMPFER box. The PGI-box is a multi-functional setup with several plug-in modules, containing e.g. a DC current source, differential amplifiers and a current meter. In this work the PGI-box was used as DC current/voltage source and differential amplifiers have been utilized to pre-amplify the signal obtained from the investigated samples, before entering in the lock-in amplifier or the Keysight meter. The current/voltage source has the possibility for a DC and AC voltage input with attenuation factors of DC:AC of 1:10 or 1:100, respectively. As a current source, it applies a current proportional to both the DC and AC voltage applied to its inputs as per the chosen settings of 10 nA/V (minimum) or 1 mA/V (maximum) or values in between. Using only the DC input, utilizing a differential amplifier as well as the keysight meter, IV characteristics have been recorded. For measuring the differential resistance directly, a small AC signal is created using the oscillator of the SR830 lock-in amplifier. This additional AC signal can be added to the DC input and the addition of the two signals will be applied to the sample. By locking the AC signal from the devices to the AC output of the SR830 lock-in the differential resistance is determined by comparing the amplitude of the two AC signals. The output of the source function chosen on the PGI-box is connected to the sample via a MATRIX-box (see Fig. 13.2). It consists of 20 sockets, each of which is connected to one of the 20 DC lines from the 12-pair loom cable. The same setup is used to process the output signals from the sample. The current/voltage readings pass one of the differential amplifiers within the PGI-box and go forth to the external measurement equipment.

The STAMPFER box was used for most measurements in this work. As in the case of the PGI-box, this also consists of an AC and DC voltage input. The relative attenuation factors here are fixed as 10000 for the AC input and 100 for the DC input. It is equipped with two ampere-meters to measure a current signal. On the STAMPFER Box's output this measured current signal will be displayed as a voltage signal which scales linearly with the current. The amplification factor at this output can be chosen from 0.1 nA/V until 10 uA/V in steps of 10. The choice of the amplification depends on the magnitude of the current values and the accuracy desired. More details about the kind of cables used, the grounding mechanism, internal components of the individual devices can be found in[43].

13.4 Schematic of the electric circuit

13.4.1 Current driven 4 point measurement

In this measurement, an AC current I_{AC} , generated using the internal oscillator of an SR830 lock-in amplifier connected to the PGI-Box's current source, is applied to the outer contacts on the NW and the corresponding potential drop across the across the inner contacts is measured. Similarly, I_{DC} can be generated using the HP Universal source connected to the current-source of the PGI-Box too. The Fig. 13.2 depicts the schematic of the measurement setup.The PGI-box when operated as an I-source gives an output-current, which is defined by the source's conversion factor chosen (for e.g., for 100 nA/1 V, a current of 100 nA will be generated at the output for every 1 V of input). It can provide a solely DC or AC or a combination of AC and DC current. The signal from the NW's inner contacts is fed back to the lock-in amplifier, which filters any but the originally applied frequency of the generated current input from the signal. The measured voltage signal from the NW was fed into the PGI-Box's differential amplifier. Here the signal is amplified according to the conversion settings chosen (for e.g., for this measurement, a gain of 1000 was chosen). This amplified signal is then displayed on the Agilent and read out by the measurement software. The amplitude of the locked AC voltage is measured and displayed on the Keysight voltmeter. The lock-in amplifier has been chosen for these measurement as it can resolve smaller signal changes than using the DC setup used for the cooldown 4-point measurement to determine the temperature dependence of the resistance of the NW.

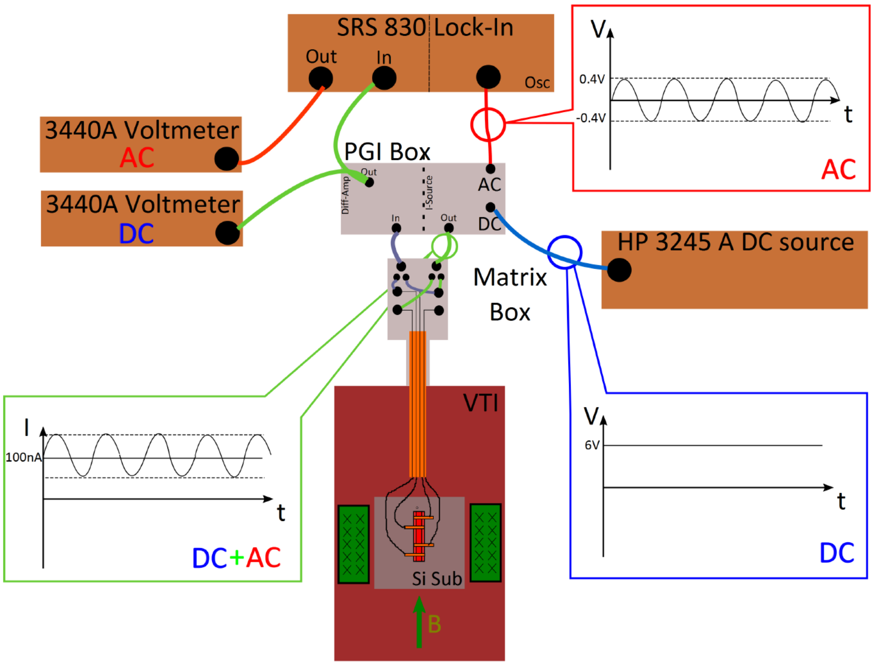

Figure 13.2: Schematic of a current driven 4-point measurement using the STAMPFER box. The setup shows an input of I_{AC} or I_{DC} or a combination of both, depending on the type of measurement, supplied to the NW and the corresponding read-out of the output V_{DC} and differential conductance dI/dV

13.4.2 Voltage driven 2 point measurement

In this measurement, a DC voltage V_{DC} as well as a relatively small AC voltage V_{AC} is supplied to the NW. The main reason behind sending a mixed DC and AC signal is to facilitate a direct measurement of the differential resistance. Thus, very small changes in the IV characteristics can be easily detected. The Fig. 13.3 depicts the schematic of the measurement setup. Here, the PGI box is replaced with the STAMPFER box and the NW is measured in a 2 point setup. A DC voltage of 6 V from the HP Universal source along with an AC voltage with an amplitude of 0.4 V and 23.3 Hz frequency is fed to the STAMPFER box. Its default attenuation factor for DC input signal is 1/100 and for the AC input signal is 1/10000. This means a total of 60 mV DC with a 40 mV of AC voltage is supplied to the sample. The corresponding output signal is then fed via the STAMPFER box into the Lock-in amplifier where the signal is filtered with respect to the frequency of the input signal. Two Keysight voltmeters display the DC part of the output signal at each contact and one displays the AC amplitude of the signal. The output is displayed as a voltage according to the conversion settings chosen on the STAMPFER box (for e.g., 100 nA/1 V means for every 100 nA of current detected, the Keysight voltmeter will display 1 V).

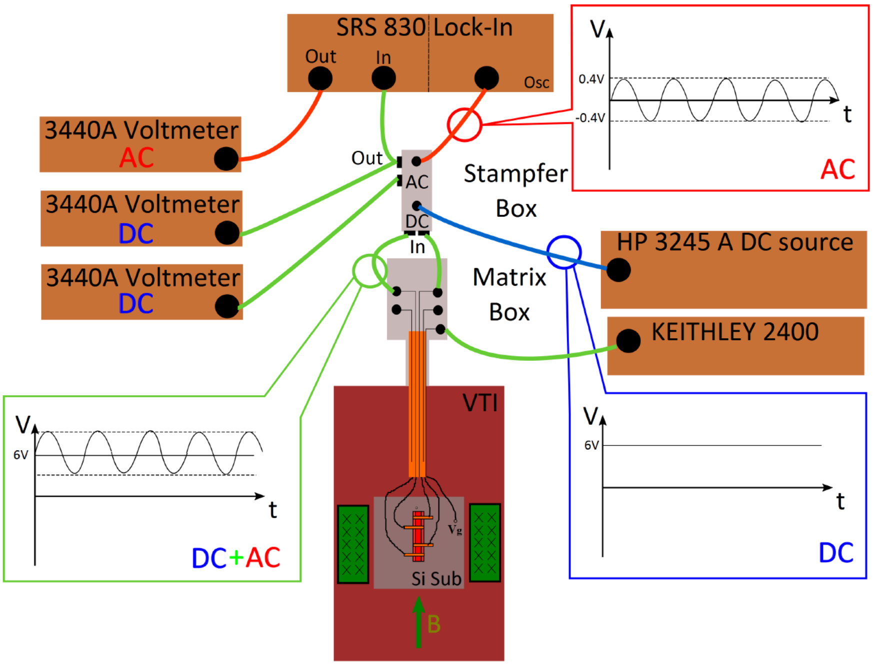

Figure 13.3: *Schematic of a current driven 2 point measurement using the PGI box. The setup shows an input of* V_{AC} *or* V_{DC} *or a combination of both depending on the type of the measurement, supplied to the NW and the corresponding read-out of the output* V_{DC} *and differential conductance* dI/dV

14 Measurements on InAs/GaSb core/shell NWs with partially etched shell

14.1 IV characterization

In this section, the electrical characterization of partially etched InAs-GaSb core-shell NWs will be presented and discussed. For these measurements, a sample consisting of NWs with a C-doped GaSb shell was used. The intended doping concentration was $6.25 \times 10^{18}\,\mathrm{cm}^{-3}$ calibrated as for GaAs layers. The NW under investigation is approximately $3\,\mu$m long with an InAs core diameter of 90-100 nm and a GaSb shell thickness of 25-30 nm, which results in an overall diameter of approximately 150 nm. As a preliminary analysis, current-voltage (IV)characteristics were measured first at room temperature using the setup described in the previous section.

Fig. 14.1 (a) displays the NW device that was used for this purpose. The Fig. 14.1 (b) shows the configuration of the contacts on the NW. The contacts are as labeled and the individual IV characteristics of each pair of these contacts is discussed by referring to these labels. Contacts 1 and 2 lie on the GaSb shell, contacts 4, 5 and 6 lie on the InAs core and contact 3 lies on the partially etched part of the NW shell. This means there were still some GaSb remnants on the NW caused by under-etching (refer section 8.2).

2-point, voltage driven measurements were performed on each pair of contacts using the STAMPFER box. Fig. 14.2 displays the room temperature measurements. The purpose of this measurement was to check if the contacts provide an ohmic contact to the sample. It was observed that only the contacts on the GaSb shell (contacts 1 and 2 in Fig. 14.1) showed perfectly linear current to voltage characteristics. The resistance for this measurement is determined with a linear fit to the curve and calculating the slope. It showed a resistance of $7.157\,\mathrm{k}\Omega$. Since, this is a 2-point measurement, this value is a sum of the resistance of the NW, the contact resistances as well as the resistance incorporated into the circuit due to the wiring and the RC filters used (value of $2.1\mathrm{k}\Omega$ per line). The source drain voltage V_{sd} was only swept from -17 mV to +17 mV since even with such low values the corresponding current values exceeded $2\,\mu$A.

The current measured for contacts on the InAs core show relatively lower values for voltages as high as 0.5 V. Thus these were measured in a range of -0.5 V to +0.5 V. For the same measurements between contact 5-4 and 5-6, which lie on the InAs core, a linear regime limited only to small voltages in the order of 50 mV was observed. At higher voltages, this

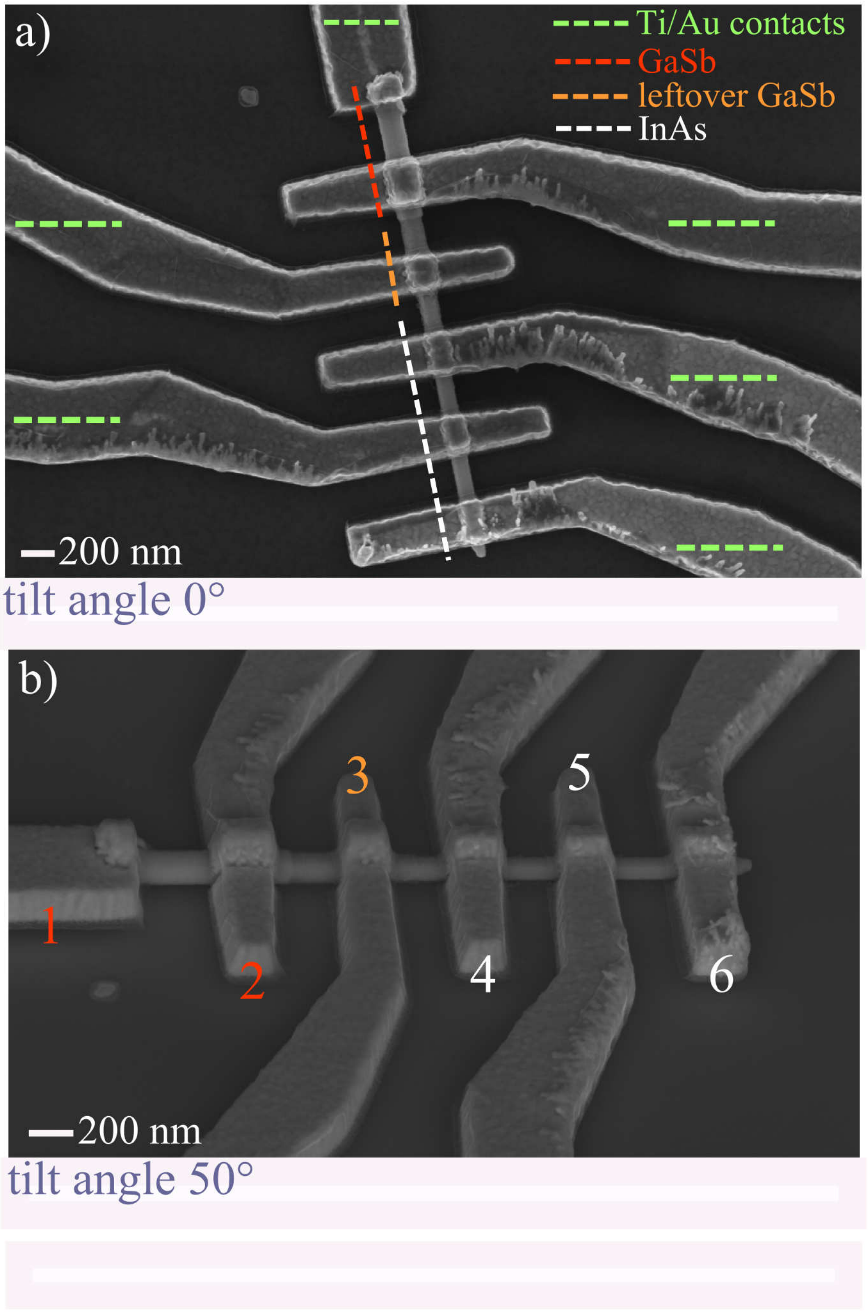

Figure 14.1: *(a) Top-view of the partially etched InAs/GaSb core/shell NW on a T-Gate substrate. Ti/Au bilayer metal contacts are placed on several parts of the NW for IV characterization. (b) the same NW at a tilt angle of 50° for a better view of the etched and non-etched parts of the NW. All materials are color-coded in (a) and color and number-coded in (b) for reference.*

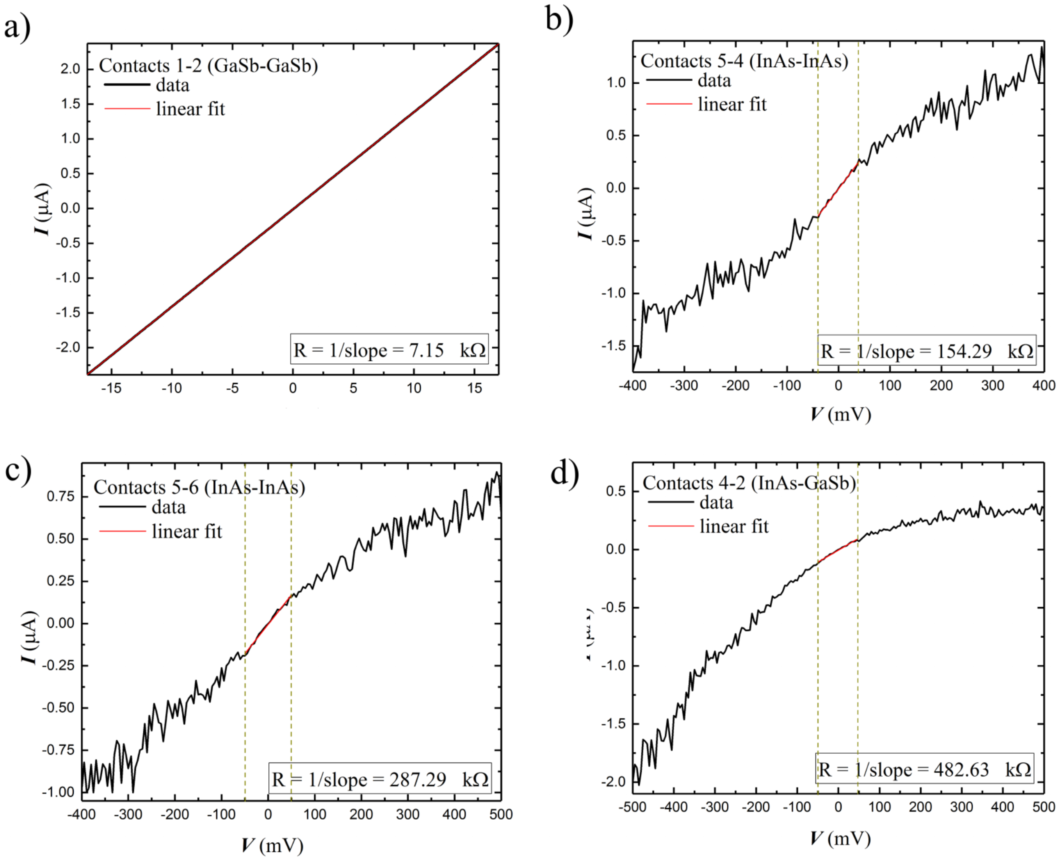

Figure 14.2: *IV characteristics of various parts of the partially etched NW. The numbers denoting the contacts are as labeled in Fig. 14.1. (a) shows a linear behavior for GaSb-GaSb, (b) and (c) show mostly linear behaviour for InAs-InAs and (d) shows non-linearity for InAs-GaSb. Linear fits is the regions highlighted are performed to estimate the order of resistances and are correspondingly displayed in the insets.*

quickly transforms into a non-linear behavior. A linear fit of the IV curve in the linear range was performed to estimate the resistance. Fig. 14.2 displays these values in the insets for the corresponding contacts. As seen, the values for resistance are much higher, i.e., in the range of several hundred kΩ. Since the value of the resistance induced by the filters has a constant value of 4.2 kΩ, the reason for such high values can be explained by either the contact resistances being too high or the InAs core being highly resistive or due to remnants of GaSb on the NW. In the first case, a bad contact between the NW and the metal layer means that there are very few points of actual contact between them. Thus, on application of higher voltages, the heat dissipation can only occur at the actual points of contact. Since these are few, the heat produced locally will have to be distributed amongst a much smaller effective area of contact. For the second and third case, it should be considered that the NW shell was etched to have access to the InAs core. The EDX measurements were not 100% conclusive about the removal of the GaSb shell completely from this part of the NW. The roughness observed with the SEM images of these etched NWs could either indicate a slight etching of the InAs core, which would definitely lead to changes in its surface states, or it could also indicate the presence of a slight GaSb layer even after etching which could also change the transport characteristics drastically. Another possibility could be the presence of native oxide even after Ar-sputtering (refer section 9.2) which could have only been successful on the GaSb part of the NW and not the InAs. Since the IV characteristics of these contacts still show a linear regime for small voltages, it is highly unlikely that the non-linear behavior is a result of the noise induced by the measurement setup.

The Fig. 14.2 (c) displays the IV characteristics between contact 2 (on GaSb shell) and contact 4 (on InAs core). The IV sweeps in between contacts 2 and 3 and contacts 3 and 4 revealed a resistance to be in the range of GΩ. This means that the contact resistance at contact 3 is higher than any other contact. The presence of a metal contact (number 3) in between the contacts that are being probed (number 2 and 4) influences the transport between these contacts. However, in this case, this influence is negligible since a resistance of GΩ implies there is hardly any contact with this part of the NW at all. The IV curve resembles diode-like behavior. This could be due to the contacts being diode-like or that the NW functions as a diode with a p-type shell and an n-type core. In order to deduce more from such measurements, they would need to be performed on many more samples to eliminate the source of the non-linear IV characteristics for the InAs part of the NW.

14.2 Back-Gate dependency

After the room temperature measurements, the sample was cooled down to 1.5 K. At base temperature the next step was to measure the Back-Gate (BG) dependency of this NW in the linear regime. The BG voltage was supplied using an additional Keithley 2400 as shown in Fig. 13.3. An ambipolar transport is to be expected due to the presence of an electron and hole gas at the hetero-interface. Thus, by measuring the influence of an external gate

Figure 14.3: *A schematic of a partially etched InAs/GaSb NW placed on T-Gate substrate that is covered with 150 nm of* SiO_2*. This* SiO_2 *layer serves as a BG dielectric.*

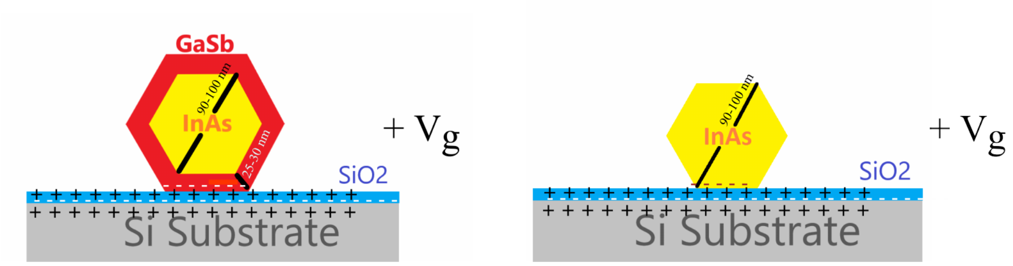

Figure 14.4: *Schematic of the NW in contact with* SiO_2 *BG substrate layer. The hexagonal morphology is highly exaggerated especially since etching the NW does not retain this for the exposed InAs part of the NW. On the left, the GaSb shell of the NW is shown and on the right the InAs core of the NW is shown. On external application of the voltage to the* SiO_2 *layer, charges are induced as shown.*

voltage V_g on the current flowing through the NW, we can deduce the type of charge carriers involved in the transport. The gate dependency was measured for both the core and the shell of the NW as displayed in Fig. 14.5.

Fig. 14.3 shows a schematic of the NW geometry with respect to the SiO_2 i.e., the substrate gate layer underneath. Since the NW is partially etched, the BG is highly asymmetric with respect to the NW profile. In regions of the NW where the GaSb shell still exists, the NW is maximally in contact with the BG. The bottom of the NW which consists only of the InAs core and does not resemble the hexagonal morphology anymore but a rather circular one. Thus, only the very small bottom section of the NW is in contact with the BG. The rest of the NW, is mostly not in direct contact with the BG. This is due to the fact that the etched part of the NW is greater than the non-etched part.

GaSb Shell: With a constant supply of 60 mV to the contacts on the GaSb shell, the BG voltage was slowly increased in steps on 10 mV from 0 V to 50 V in order to avoid quick charging and discharging of the BG layer. Fig. 14.5 (a) shows the BG sweep that was conducted from +50 V until -30 V. As displayed, a relatively high current of approximately 4 μA is measured. For increasing BG voltage, the corresponding source-drain current I_{sd} shows a decline. This is an indication for p type behavior. This can be understood with the

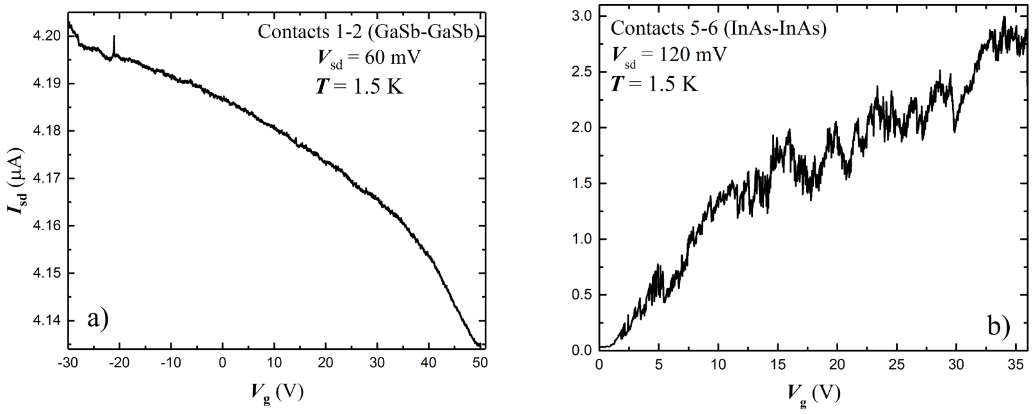

Figure 14.5: *(a) Shows the back-gate voltage dependency of the GaSb shell of the NW. A decreasing I_{sd} with increasing positive gate voltage V_g implies p-type behavior. (b) Shows the back-gate voltage dependency of the InAs core of the NW. An increasing I_{sd} with increasing positive V_g implies n-type behavior.*

schematic showed on the left in Fig. 14.4

A positive V_g applied to the substrate will attract negative charges at the SiO_2/Si interface within the oxide layer. Due to this orientation of the dipoles within the oxide layer, charges in the oxide itself will compensate, while leaving the oxide interface to the NW positively charged. This will in turn attract negative charges within the NW towards the NW to oxide interface. Thus, with the applied source-drain bias V_{sd} of 60 mV, there is a current I_{sd} of approximately 4 μA flowing across these contacts on the NW. An additional supply of a positive V_g induces negative charges at the NW-SiO_2 interface. Since the I_{sd} shows a decrease due to this applied positive V_g, this implies that the induced negative charges reduce the amount of majority carriers. And since these are negative charges, the majority carriers are holes. This confirms that the C-doped GaSb shell is indeed p-type. The relatively low decrease in I_{sd} even with very high positive V_g indicates that the GaSb is heavily doped. This means that V_g did not have much influence over the transport of the charged carriers. This implies that the amount of dopants is very high and they control the transport through the NW. Although no full pinch-off obtained to be able to estimate the carrier concentration, the measurement at least confirms the high doping of the GaSb shell.

InAs core: The schematic on the right in Fig. 14.4 shows the InAs core in contact with the BG substrate layer and due to the mechanism described for the shell, a positive V_g induces negative charges in the NW at the NW/SiO_2 interface. A V_{sd} of 120 mV is applied on the contacts 5 and 6. However, this time an increase in the I_{sd} was observed which implies n-type behavior in the InAs core (refer to Fig. 14.5 (b)). This measurement could not be repeated to check if the position of the oscillations remain the same or not. The nature of the curve can only be attributed to UCFs if this measurement could be repeated. The observed BG response can also attributed to bad contacts on the InAs core of the NW.

However, the general increasing trend of the I_{sd} confirms that the InAs core is indeed n-type. Unfortunately, due to electrical discharge, this sample could no longer be used to investigate the influence on the BG on the transport between contacts 2 and 4, i.e., the transport at the hetero-interface.

Thus, due to the good ohmic contacts observed to the GaSb shell on the NW and the confirmation of the n-type and p-type behavior of the InAs core and the GaSb shell respectively, further measurements were conducted on non-etched InAs/GaSb core/shell NWs.

15 Measurements on non-etched InAs/GaSb core/shell NWs

In this section, the electrical characterization of InAs/GaSb core/shell NWs will be presented and discussed. For these measurements, a sample consisting of NWs with an un-doped GaSb shell was used. The NW under investigation is approximately 4 μm long with an InAs core diameter of 90-100 nm and a GaSb shell thickness of 25-30 nm, which results in an overall diameter of approximately 150 nm. The Fig 15.1. shows the NW that was under investigation in this section. The samples consisting of non-etched NWs showed good ohmic contacts with measurements showing resistances in the range of a few kΩ. This will be described in more detail in the following section. Thus, this sample was chosen to conduct magneto-transport measurements on.

15.1 Cooldown and IV sweep

After mounting the sample onto the dipstick, at room temperature, all contacts were checked to be working. Then, once the sample was placed in the cryostat, the resistance as a function of temperature was measured. This was done using a 4-point measurement setup described in section 13.4.1. A constant current is supplied across the outer contacts (as labeled in blue in the Fig. 15.1 and the potential drop across the inner contacts (as labeled in pink in the Fig. 15.1) is measured. The setup used for this measurement and for the measurements performed on the NW in this section is schematically represented in Fig. 13.2. An HP 3245A constant voltage source of 1 V output was used as a voltage input to the PGI-box's current source. In this case, I_{DC} of 100 nA was then supplied to the NW constantly, while the temperature is varying from 160 K until 1.5 K. The temperature rate is defined by operating the needle valve connecting the dewar and the sample chamber in the VTI. The resistance as a function of temperature can be defined using the measured potential drop displayed on the Keysight voltmeter (taking the amplification factor of the differential amplifier into consideration) and dividing it by the constant current applied on the outer contacts. Fig. 15.2 displays the resistance measured in the four point setup as a function of temperature. Due to this setup the values recorded are solely that of the NW and do not have a contribution from the contact resistances or the resistance from the electrical components.

As observed, the resistance shows an increase with decreasing temperatures. This behavior confirms the semiconducting behavior of the core/shell NWs. The resistance of a semiconductor depends on the carrier concentration as well as the mobility of the carriers.

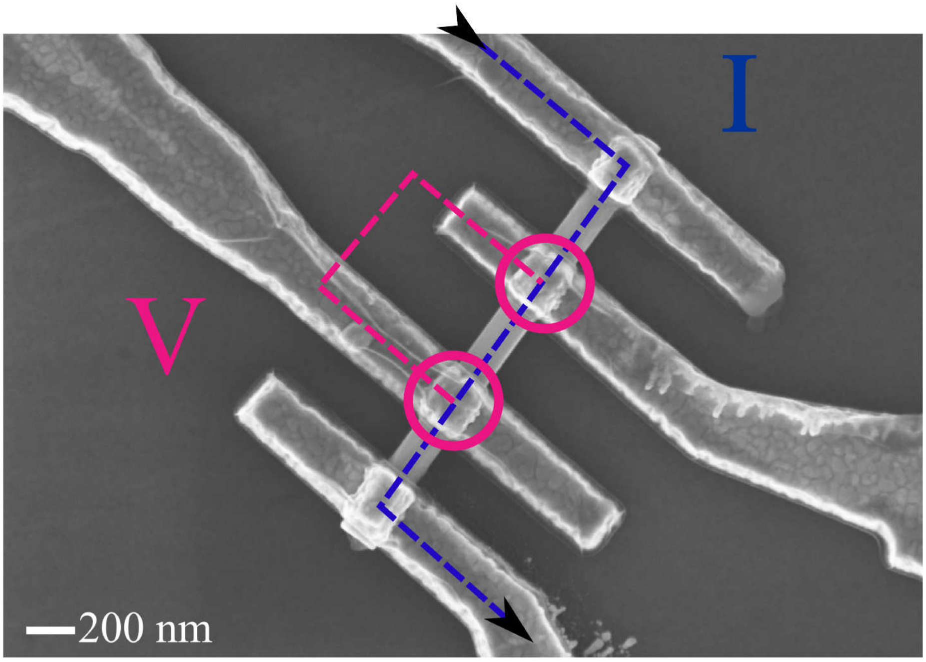

Figure 15.1: *The InAs/GaSb cores/shell NW measured in a 4-point measurement setup described in section (13.4.1). The current I is supplied across the outer contacts (labeled blue) and the corresponding voltage drop is measured across the inner contacts (labeled pink)*

These, in turn, are temperature dependent based on the dominant scattering mechanism. Lower temperatures would possibly freeze out carriers and would lead to decreased conductance. The InAs/GaSb core/shell NWs are a complex material system comprising to two semiconductors. Thus, the temperature dependence deviates from the more simplistic macroscopic single semiconductor picture. However, the general trend of increasing resistance with decreasing temperature is still observed and the anomalies in the curve can be attributed to the fact that this is a nano-scale complex material system.

Next, a current driven IV sweep was performed by varying the current across the outer contacts on the NW from -100 nA to 100 nA and the corresponding voltage drop across the inner contacts was measured. This is displayed in the Fig. 15.3. As seen, a slight non-linear behavior is observed around small values of the current. Two separate linear fits are performed to determine the resistance of the NW as displayed on the curve itself. Since this is a four point measurement, the values correspond to the resistance of the NW itself.

One possible explanation for this behavior is if the NW picture is simplified to a p-n junction diode. Here, we assume the GaSb shell to be p-type (since it is not intentionally n-type doped and even has a small p-type background doping due to the MBE system). The InAs core is n-type and thus the interface between these two materials can be thought of as a depletion layer in a p-n junction diode. This is schematically depicted in Fig. 15.4. The two materials of the NW provide some resistance which would effectively be parallel to each other connected via the diodes. Here, the current flowing just through the GaSb shell

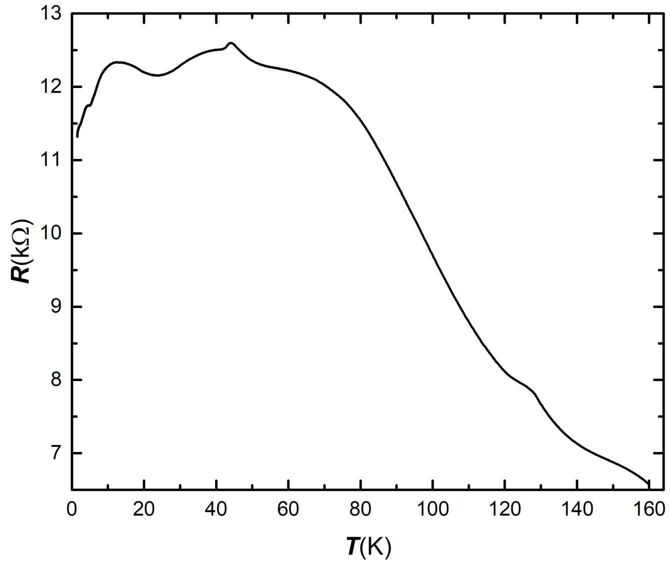

Figure 15.2: *The temperature dependence of the InAs/GaSb core/shell NW resistance in a 4-point current driven setup is displayed. The general trend of increasing resistance with decreasing temperature confirms the semiconductor behavior of the NW.*

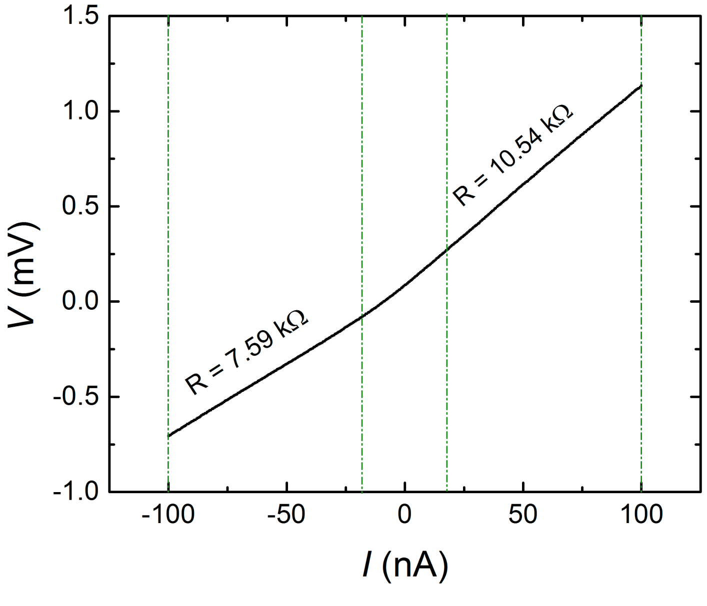

Figure 15.3: *IV characteristics of the InAs/GaSb core/shell NW in a current driven 4-point measurement setup. Two linear fits are performed as displayed to determine the corresponding resistance values R. The possible explanation for the slight non-linear behavior is described in section 15.1*

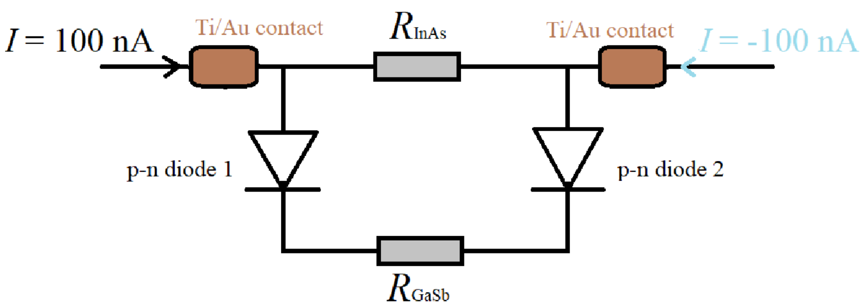

Figure 15.4: *Schematic of the very simplified diode picture of the core/shell NW. The interface between the InAs core and the GaSb shell as a p-n junction, and the resistance contribution from both materials as* R_{InAs} *and* R_{GaSb}*. The area of the NW under consideration is in between the inner lying Ti/Au contacts.*

to the contacts is neglected. If the two diodes were perfectly symmetric, then the IV curve is expected to be perfectly symmetric irrespective of the polarity of the driving current I_{sd} supplied in between the contacts. However, the non-linearity caused due the reversed polarity of I_{sd}, implies that the current flow is more favorable in one direction than the other, leading to a decrease in resistance.

This would imply that the charge transport definitely occurs in the InAs core along with the GaSb shell through the interface. To be able to further investigate this, measurements to determine the temperature and angle dependence of the magneto-conductance were performed next.

15.2 Magneto-transport

In this section, the transport characteristics of the NW with respect to an applied magnetic field is discussed. Since an ambi-polar transport mechanism is expected from this material system, the effect of an external magnetic field on the conductivity can be of use to understand the contributions of both materials to the overall transport. In[44] magneto-conductance measurements on GaAs/InAs core/shell NWs at different tilt angles between the NW axis and an external magnetic field direction was measured. This was analyzed in great detail experimentally and theoretically to show how angle resolved measurements can be used to resolve electron motion in NWs. Following this work, a similar attempt was made to investigate these NWs, which, as opposed to the type-I band alignment of GaAs/InAs, are expected to have a type-III broken gap alignment. Similar measurements performed in this section will shed some light on the results obtained and provide a possible explanation for the distribution of charge movement in the InAs/GaSb core-shell NWs. The sample was intentionally glued onto the chip in such a way that the direction of the magnetic field applied within the cryostat would lie in-plane and parallel along the NW axis. This was to be able to measure possible Aharonov-Bohm or Alts'huler-Ahronov-Spivak interferences within the NWs cross section. The rotating sample holder would also facilitate a perpendicular alignment between the NW and the applied magnetic field.

15.2.1 Temperature dependence of magneto-conductance

The temperature dependency of magneto-transport measurements can help to estimate the temperatures until which phase coherent transport can be observed. This is because at low temperatures due to less thermal energy supplied to the system helps reduce inelastic phonon scattering. Thus, assuming a diffusive, phase coherent transport, electron interference effects can be observed and analyzed. In[31] work, these types of measurements were performed to determine the phase-coherence length of the carriers in InAs, InN NWs as well as InAs/GaAs core/shell NWs. Although, evidently, these material systems are not comparable to InAs/GaSb, the mathematical and statistical methods harnessed to analyze the measurements were used as a reference.

In the case discussed here, the sample is oriented in a way that the magnetic field will be applied parallel to the NW axis. With a particular constant temperature T(K) and constant current I_{AC} of 10 nA applied, the magnetic field was swept from -13 T to 13 T and the corresponding potential drop across the NW was measured in the 4-point measurement setup described in the section 13.4. The reason for such a small magnitude of I_{AC} is to reduce thermal energy provided to the NW that may be caused due to high currents, potentially reducing quantum interference effects due to local heating effects. This was repeated for increasing temperatures starting from a base temperature of 1.5 K until 50 K. The temperature in this range is varied using the heater mechanism described in the section 13.2. The Fig. 15.5 shows the magneto-conductance in the units of the conductance quantum as a function of varying magnetic field for temperatures from 1.5 K until 50 K.

An applied parallel magnetic field will force electrons to circular motion on 2D planes in the NW cross-section. The applied current bias will result in these circular orbits to have a rather helical nature oriented along the NW axis. Scattering of the electrons can however form any kind of 3D closed loops for electrons to interfere with themselves (Aharonov-Bohm effect or Alts'huler-Ahronov-Spivak effect). Depending on whether they interfere constructively or destructively, a corresponding increase or decrease in the quantum mechanical probability to find the particle at the loops origin can be observed. Mesoscopically this will lead to an observable change in the NW conductance as explained in the theory section 1.5. Due to the parallel magnetic field alignment, electrons traveling along the scattering dependent interference loops will be influenced by a vector potential, that alters the phase of the electrons proportional to the magnetic flux penetrating the loops. Due to the possibility to form any kind of given 3D shape of these interference loops not only closed loops on the cross-sections perpendicular to the applied magnetic field needs to be considered but any 2D projection of the 3D loops onto these planes. While a single loop or a 2D projection will lead to periodic changes in the mesoscopic conductance, a set of loops will result in an observable spectrum of quantum interference oscillation, which is superimposed with the sample's mesoscopic behavior.

All the analysis carried out in this section in based on the theory presented in Quantum

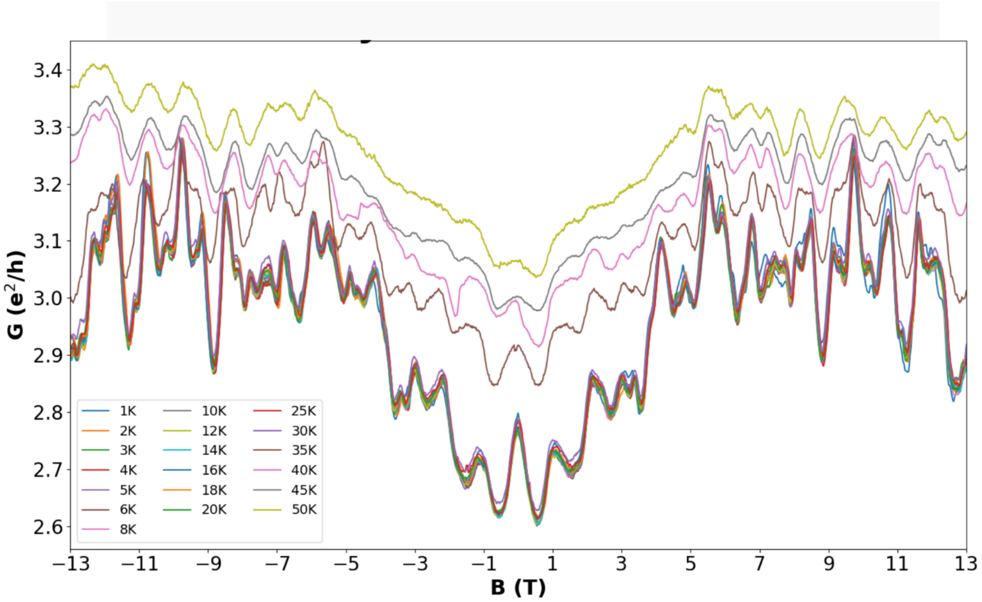

Figure 15.5: *The figure displays magneto-conductance G as a function of magnetic field for temperatures varying from 1.5 K until 30 K*

transport in semiconductor nanostructures[29, 30]. This has been briefly discussed in the section 1.5 in the theoretical background presented at the beginning. Similar analysis was carried out for different material system in the work of [31] and was also used as a reference. From Fig. 15.5, it can be observed that the magneto-conductance G fluctuation pattern follows the same pattern from temperatures ranging from 1.5 until 30 K. However, the fluctuation amplitudes reduce for higher temperatures. The fluctuations observed are a combination of fluctuations caused in the system due to classical mesoscopic properties (background conductance) which are superimposed with contributions from to quantum effects. Thus, for further analysis, a deviation of conductance G from the average value, i.e., the background conductance, is calculated. A more mathematically robust way of explaining this is calculating the deviation of conductance as a function of the magnetic field using:

$$\delta G(B) = G(B) - < G(B) > \tag{15.1}$$

This is done to remove the background contribution to the G and thus only obtain the magnetic field dependence change in G due to the electron interference effects. After subtracting the background contribution, fluctuation amplitudes are presented in Fig. 15.6.

From this data the average fluctuation amplitude is calculated as:

$$\mathrm{rms}(\delta G) = \sqrt{< (\delta G)^2 >} \tag{15.2}$$

This is displayed as a function of temperature in Fig. 15.7. As analyzed from the Fig. 15.7, the average fluctuation amplitude is nearly constant for temperatures ranging from 1.5 K until 30 K. This is an indication that even with additional thermal energy provided to the system, the phase-coherent transport among a certain set of interference loops is retained

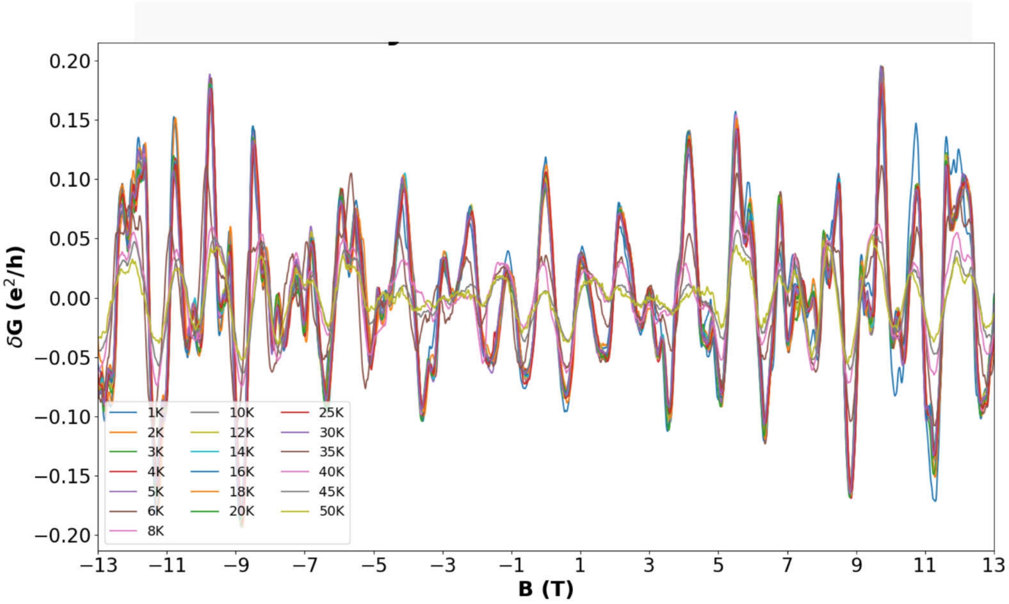

Figure 15.6: *δ G(B) dependence on the magnetic field for varying temperatures (from 1.5 K until 30 K). These fluctuation amplitudes are purely due to contributions from electron interference effects.*

until 50 K. Thus, it can be deduced that in this temperature range, the transport is only limited by the sample dimensions i.e., the length and diameter of the NW, since the phase coherent transport is maintained even with some additional thermal energy.

The phase coherence length, l_ϕ, along with the thermal length, l_T together with the diffusion constant determine the rms(δG). An estimate of both these length scales cannot be performed without measuring the temperature dependency of the magneto-conductance in different orientations of the angle of the magnetic field. However, it can definitely be concluded that due to constant value of the rms(δG) in a temperature range of 1.5 K to 30 K, both l_ϕ and l_T exceed the sample dimensions.

The sudden decrease in the rms(δG) in the temperature range of 35 K until 50 K suggests that both l_ϕ and l_T both are now smaller than the sample dimensions. The overall average G increases with increasing temperature due to the additional thermal energy available to the electrons mesoscopically. This can be understood in the following way with the brief explanation of Thouless energy E_{th}. In a confined state of a particular dimension, E_{th} is the measure of the energy of the state and the phase development. A phase is gathered by a wave across the conductor while propagating. Considering the phase difference between two different waves with slightly different wavevectors, the energy required for them to have a phase difference $\Delta\phi = 1$ is the Thouless energy. Thus, it is also a measure of the correlation energy, i.e., the energy difference between two uncorrelated states. Thus, for temperatures above 30 K, a thermal averaging occurs for the electrons. The energy distribution of these electrons exceeds the energy spacing of the energy levels defined across the dimension of

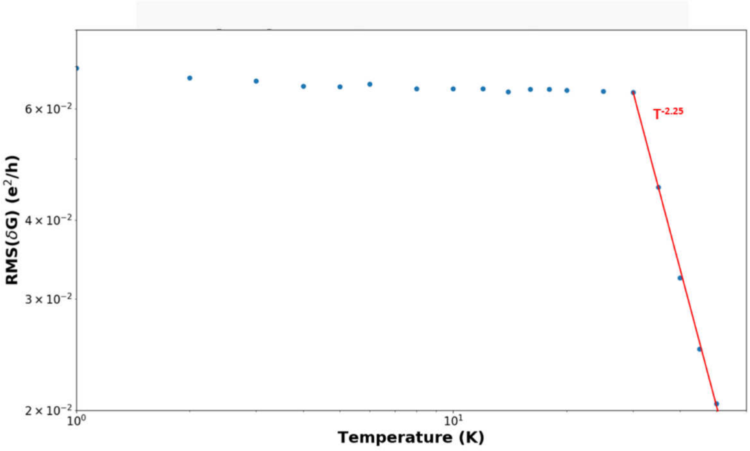

Figure 15.7: *rms(δG) as a function of temperature. A saturation region is observed for a temperature range of 1.5 K until 30 K. For higher temperatures, a rapid decay in the rms(δG) value is observed.*

the conductor and the de-coherence caused due to the correlation between adjacent energy levels, is possibly the reason for the decrease in the average fluctuation amplitude.

It should be noted that the fit performed for the temperatures above 30 K results in a exponent value which is far larger than obtained from theory. From this analysis, it was concluded that phase-coherent transport occurs in the NW for temperatures below 50 K with l_ϕ becoming smaller for temperatures above 30 K. Thus, with the angle dependence of G at temperatures below 30 K, more information about the size and location of the electron interference loops can be determined. This will be discussed in the subsequent section.

15.2.2 Angle dependence of magneto-conductance

As the previous section, all the analysis carried out in this section in based on the theory presented in Quantum transport in semiconductor nanostructures[29, 30]. This has been briefly discussed in the section 1.5 in the theoretical background presented at the beginning. Similar analysis was carried out for different material system in the work of [31] and was also used as a reference.

As described in the section 13.2, the dipstick is equipped with a stepping motor that allows for changing the angle between the sample and the applied magnetic field by rotating the sample holder. Thus, 4-point measurements with the same electrical setup described in the section 13.4 were conducted on the sample at the base temperature of 1.5 K. Thus, the effect of thermal averaging as described in section 15.2.1 can be neglected. The magneto-conductance G was measured as a function of varying angles between the sample and the magnetic field. Since the dipstick was mounted with the NW axis aligned aligned with the magnetic field, the measurement was repeated for several angles varying from the initial 0° (in-plane parallel) magnetic field orientation until 100° degrees (where 90° corresponds

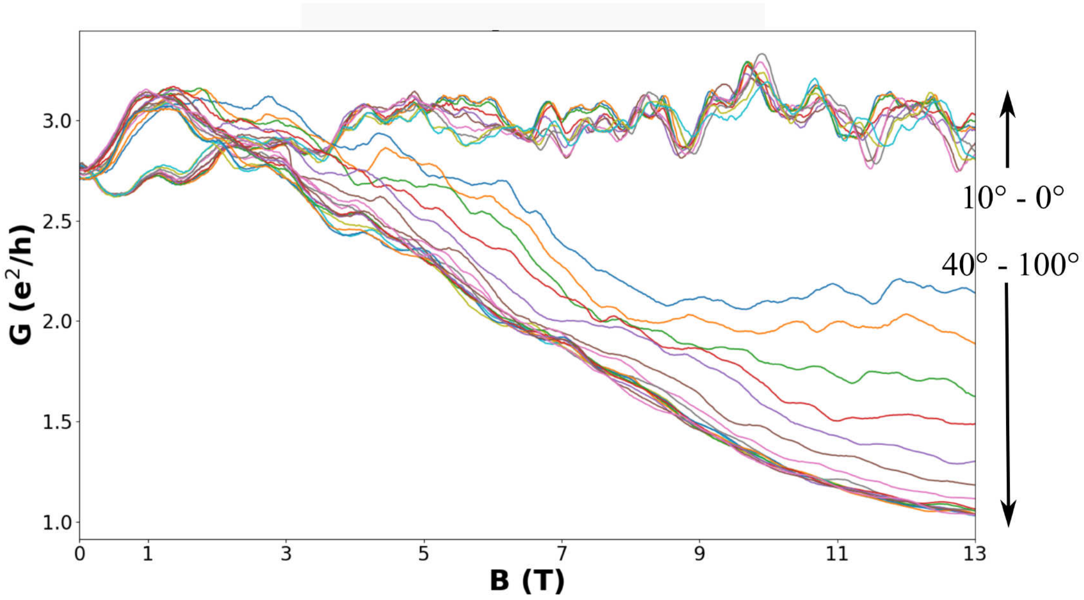

Figure 15.8: *Angle dependency of magneto-conductance G as a function of the magnetic field, for varying tilt angles*

to the magnetic field out of plane, perpendicular to the substrate, orientation). For each of these orientations, the magnetic field was now swept from -13.75 T to 1 T. The range of the magnetic field was reduced on account of the fact that G is symmetric around the zero magnetic field as has been proven in from the previous measurements (refer Fig. 15.5). G calculated in units of the conductance quantum as a function of the magnetic field for varying orientations is displayed in the Fig 15.8.

Starting from the same fluctuations observed in section 15.2.1, now a change in G is observed with respect to the relative angle between the NW and the magnetic field. With varying angles, the magnetic field is now projected onto effectively larger areas of the NW. The electron interference loops however, will still be the same. This can be seen for tilt angles from 0° until 10°. The fluctuations follow the same pattern with the magnetic field. Following the data analysis which requires to subtract the background contribution to obtain pure fluctuation amplitudes from section 15.2.1, the average fluctuation amplitudes for varying tilt angles as a function of the magnetic field are presented in Fig. 15.9.

Depending on the tilt angle, a change in the fluctuation pattern is observed. These fluctuations can be analyzed further to obtain an estimate on the area of the electron interference loops. This can be done by considering the following relation:

$$\phi_0 = B \times A \tag{15.3}$$

where B is the magnetic field, A is the area of the interference loops and ϕ_0 is the magnetic flux quantum. Now, the loop area can be determined by performing an FFT of the G de-

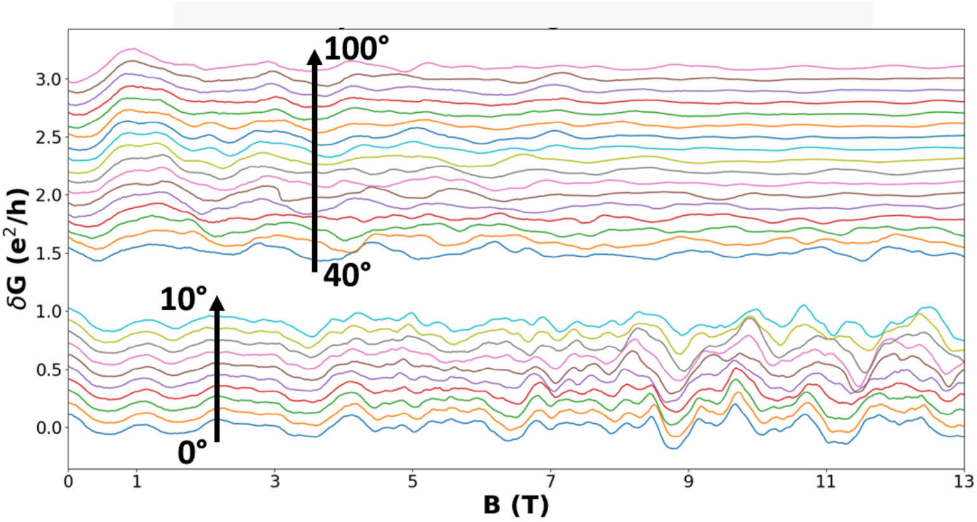

Figure 15.9: *Angle dependency of the magneto-conductance G displayed in the range of 0°-10° as well as for 40°-100°.For better visualization the single magnetoconductance traces for fixed tilt angles have a continuous offset.*

pendence on the magnetic field for tilt angles from 0° to 10°. This is displayed in Fig. 15.10. The x-axis determines the tilt angle degrees (°), the y-axis determines the area in nm^2 and the colour code is the FFT amplitude. Distinct contrasts (i.e., highest FFT amplitudes) at approximately 1×10^3 nm^2 and 1.75×10^3 nm^2 suggest that the major contributions for electrons interference effects are from these loop areas. Assuming an effectively parallel alignment of the magnetic field in this range of tilt angles, these loops can be assumed to be circular in nature and would correspond to radii of 16 nm and 23 nm.

It is also possible that a change in amplitude is not observed due to a bad resolution in the frequency spectra. This means for:

$$f_{min} = 1/B_{max} = 0.0769(1/\mathrm{T}) \tag{15.4}$$

which corresponds to an area of 1.55×10^2 nm^2. Thus, since the range of areas that are obtained are in the same range, it is not possible to resolve areas for very high magnetic fields.

For the range of tilt angles from 35° until 100°, the conductance is observed to be rapidly decreasing with increasing magnetic fields. A corresponding FFT is now performed for this range of tilt angles to determine the loop size. This is displayed in Fig. 15.11. As observed, the distinct contrast for the highest FFT amplitudes occur at areas that are much smaller than the ones obtained in the effectively parallel field alignment. A possible reason for this could be that with higher tilt angles, a higher electron scattering could be caused.

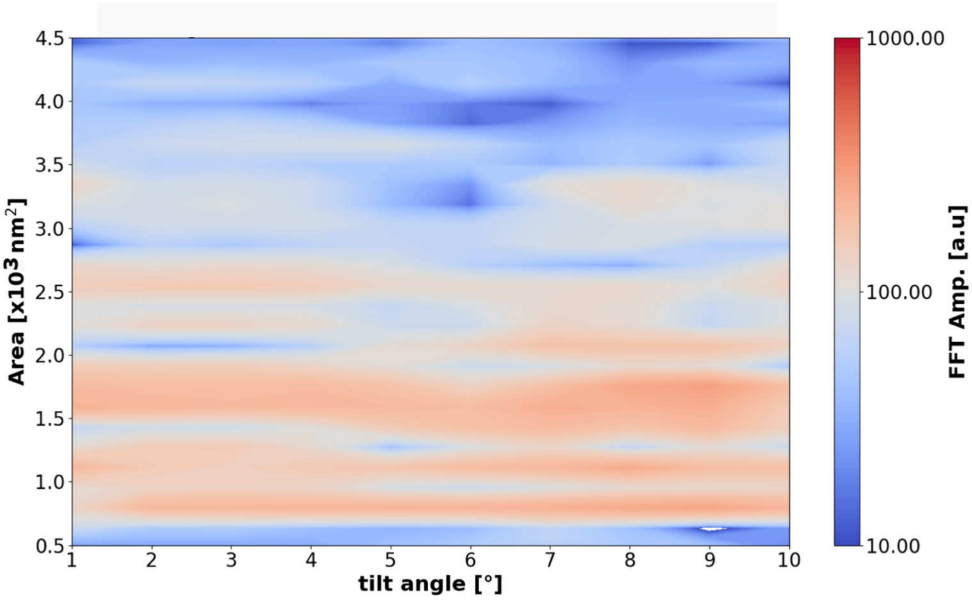

Figure 15.10: *A 2D colour plot of the FFT as function of varying tilt angles from 0°-10° and corresponding loop areas of electron interference trajectories.*

However, on comparison with the effective area of the InAs core of the NW which is approximately $6.3\times10^3\,\mathrm{nm}^2$, the areas calculated for all the tilt angles are much smaller. This can be an indication that the majority of the electron interference loops are present within the InAs core. This agrees well with the p-n diode model of the NWs that was described in section 15.1 where it was concluded that the majority of the charge transport for NW with an undoped shell indeed occurs within the InAs core.

Now, in order to qualitatively determine the phase-coherence length l_ϕ, it is assumed that the majority of the electron interference loops exist within the InAs core. In this case, it is helpful to calculate the correlation field B_c for all the tilt angles. Fig. 15.12 (a)displays these for all tilt angles. Once again, as observed with the FFT, two distinct regimes can be distinguished, one for the effectively parallel field alignment and one for the effectively perpendicular field alignment. The B_c does not vary much within these regimes. The corresponding correlation areas for the two regimes can be then estimated via the relation:

$$A_c = \Phi_0/B_c \tag{15.5}$$

These areas are displayed in Fig. 15.12 (b). Since we assume the electron interference loops to be present within the InAs core, these areas are possibly only limited by the phase-coherence length and the diameter W of the NW. It is also possible that it is restricted by the phase coherence length in both direction. Thus, an estimate from the areas for l_ϕ in both cases can respectively be obtained as:

$$A_c \propto l_\phi \times W \tag{15.6}$$

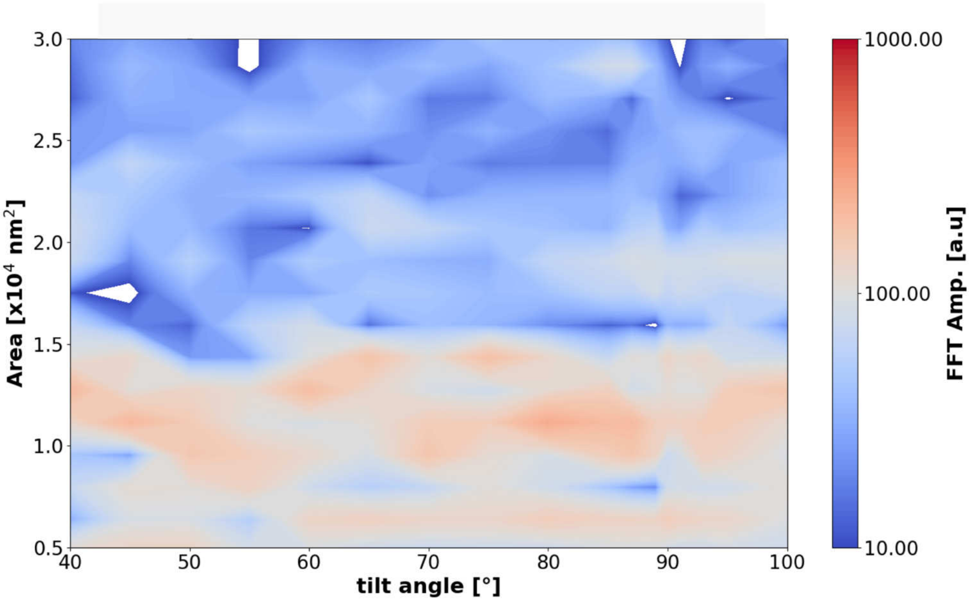

Figure 15.11: *A 2-D colour plot of the FFT as function of varying tilt angles from 40 °-100 ° and corresponding loop areas of electron interference trajectories.*

$$A_c \propto {l_\phi}^2 \tag{15.7}$$

For tilt angles ranging from 0°-10°, are approximately estimated to be $1{\times}10^4\,\mathrm{nm}^2$ and for the tilt angles ranging from 40°-100° is approximately estimated to be $7{\times}10^3\,\mathrm{nm}^2$. Thus, comparing these to the approximate areas obtained from the FFT analysis, the values do not match for the parallel field alignment, however, only within an error factor of two. Assuming the transport to be restricted only by l_ϕ, from the equation above, l_ϕ can be estimated to be approximately 100 nm. As can be observed, the effective areas are smaller for the perpendicular field alignment than the parallel field alignment. This in turn implies that l_ϕ shows a strong angle dependence by becoming smaller for increasing tilt angles. Thus, the effect of scattering is stronger for perpendicular alignment compared to a parallel alignment, possibly due to increased electron scattering.

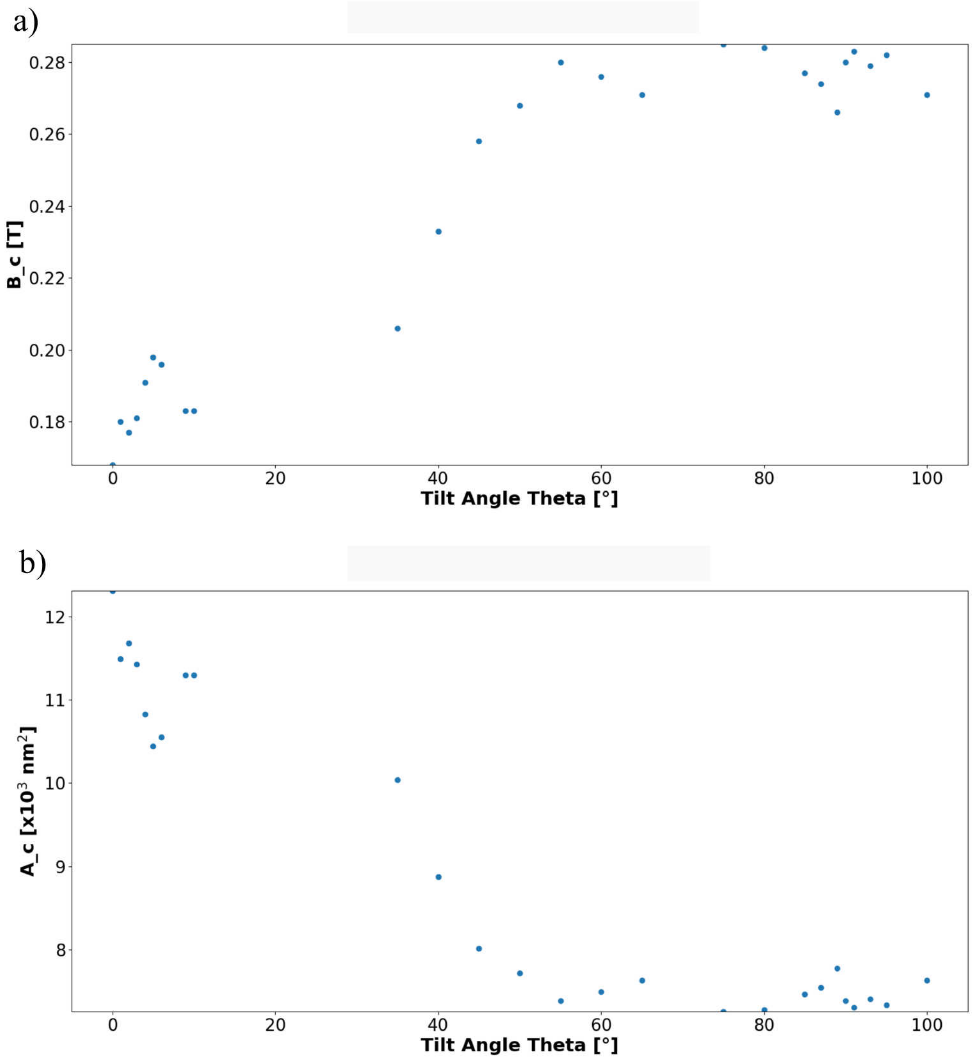

Figure 15.12: *(a) Correlation field as determined using the auto-correlation function of $\delta G(B)$ dependent on the tilt angle of the magnetic field with respect to the NW. (b) Respective correlation Area by using $A_c = \Phi_0/B_c$ dependent on the tilt angle.*

Conclusion and Outlook

This work began with the optimization of substrate preparation for selective area epitaxy of InAs and InAs/GaSb core/shell NW arrays. The pre-established process was found to be irreproducible with regards to RIE etch rates and these needed to be re-determined. Certain changes to the EBL design that defines the array pattern had to be made to increase NW yield and reduce the time required for processing these substrates. A detailed study with the help of AFM and SEM was carried out to make this process reproducible. With respect to the size of the NW, a thinner diameter was desired for better device fabrication, i.e., to have a uniform coverage of the metallic contacts around the NW. Thus the In rate and the As flux were modified during the MBE growth to obtain thinner diameter of the NW.

For proper electrical characterization, the doping of the GaSb shell was tested. Although the effects of different doping concentrations can only be meaningfully realized once the DC characteristics are compared, the effect on the morphology of the NW was presented. In order to simultaneously contact the core and shell of the NW to obtain information about the transport at the interface of the two materials, it was necessary to etch part of the GaSb shell. Wet and dry etching techniques were implemented to obtain this and the process with 0.5 M NaOH was successful.

Although a lot of time was invested in careful fabrication of these NW devices, some parts of the processes could be looked into again and optimized further. A better control over the selective etching of the NWs using NaOH can be tested out with different molarities of the solution. The dry etching technique using Cl_2 in RIE can be combined with a wet etching step to check for better reproducibility and surface quality. A comparison based on electrical characterization of several such samples can help conclude which etching leads to better ohmic contacts. Other processes for removal of the native oxide prior to metallization could also provide a basis for comparison in such measurements. Conformal deposition of the metals could also be a major contribution to obtaining better contacts on the NWs and could drastically change contact resistances. A comparative study with different metal bilayers can also to be used to conclude which material systems are compatible with both InAs and GaSb to provide better results with respect to device processing as well as measurements.

Finally, after overcoming the various technological problems, NWs both with etched and non-etched GaSb shell were successfully deposited with metal contacts. After dicing and bonding of the samples, both types of NWs were measured at room temperature as well low temperature using a cryogenic setup. A careful combination of the devices at hand was implemented to obtain 4-point voltage driven measurements and 2 point current driven measurements wherever required. DC characterization revealed the contacts on the GaSb shell to be perfectly ohmic, whereas on the InAs core were found to be non-linear. This non-linearity was attributed to possible high contact resistances, or changes caused in the surface states of the InAs core (possibly remnants of GaSb too) due to selective etching of the GaSb shell, or due to insufficient Ar sputtering to properly remove the native oxide.

Several more measurements on similarly fabricated samples need to be conducted in order to investigate the reason for this non-linearity. Thus, it was logical to conduct gate dependent measurement next to determine the type of carriers for both materials. Gate dependent measurements conducted at 1.5 K were conclusive about the InAs core being n-type and the C-doped GaSb shell being p-type.

4-point current driven measurements conducted on NWs with a non-doped and non-etched shell to determine the resistance of the NW showed an asymmetry with respect to the polarity of the driving current. This was explained using a p-n diode picture of the NW and was attributed to the asymmetry of the diodes. This asymmetry also suggested that for a NW with a non-doped shell, the majority of the charge transport occurs in the InAs core. Thus, it was concluded that to understand the charge transport in this complex material system better, magneto-transport measurements would be helpful. Since the non-etched core/shell NWs showed perfectly ohmic contacts that were placed on the GaSb shell, they were chosen to conduct magneto-transport measurements on. The temperature dependence of the conductance in a magnetic field was analyzed in detail. Due to a parallel alignment of the NW in a magnetic field spanning from -13 T to 13 T, fluctuations in the conductance were observed. Calculations of average fluctuation amplitudes show that the transport is phase coherent until 30 K and l_ϕ and l_T are only limited by the samples dimensions. Above 30 K, a strong temperature dependence suggests the lowering of the l_ϕ due to additional thermal energy in the system. This was attributed to the thermal averaging of the electron energies near the Thouless energy V_{th} leading to decoherence in the system. Following this, to locate these electron interference loops, angle dependency of the the magneto-conductance was probed. These measurements reveal a strong angle dependence of the phase-coherent length and suggest the location of the loops to be inside the InAs core.

To follow up on these results, several more measurements can be conducted on NWs with differently doped GaSb shells. A comparison of these results will definitely be more conclusive about the charge transport in this system. A top-gate can also be fabricated onto the NW to have better control over the carriers and finally, gate dependent measurements in varying magnetic fields can reveal much more about the charge transport.

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